OKI Semiconductor

FEDL2250FULL-06
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ML2251/52/53/54/56-XXX, ML22Q54/Q58

2-Channel Mixing Oki ADPCM Algorithm-Based Speech Synthesis LSI

GENERAL DESCRIPTION

The ML2250 family is a 2-channel mixing speech synthesis device with an on-chip voice data (i.e., phrases) storing mask ROM and a flash memory. Besides playing the built-in voice data, this device can output voice data that is input from outside the device. This ML2250 family allows selecting the playback method from the 8-bit PCM, non-linear 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms. And the sound volume is adjustable as well.
The ML2250 family incorporates a 14-bit D/A converter and low-pass filter.
It is easy to configure a speech synthesizer by externally connecting a power amplifier and a CPU to the ML2250 family.
The ML2250 family line-up includes 2 types of products: with on-chip mask ROM, and with on-chip flash memory.

- ML2251/52/53/54/56-XXX

This is a CMOS single chip speech synthesis device with an on-chip mask ROM. Products with 5 types of mask ROMs are available in the ML2250 family depending upon the total playback time length.

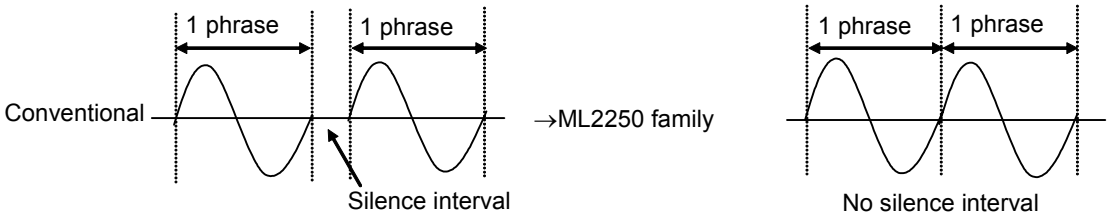
- ML22Q54/Q58

  The ML22Q54/Q58 is a speech synthesis device with a 4-Mbit/8-Mbit flash memory built in. The voice data can be easily written to the flash memory using a special tool. The on-chip flash memory product is suitable for the diversified low volume production or short delivery time applications that the on-chip mask ROM product cannot support. The ML22Q54/Q58 is most suitable for evaluation because the circuit configuration is the same as the on-chip mask ROM product.

Table below summarizes the points of difference between the ML2250 family and currently manufactured products with a ROM built in.

	ML2250 family	MSM6650 family	MSM9800 family	ML2210 family
Interface	Parallel or serial	Parallel, serial or stand-alone	Parallel or stand-alone	Serial
Playback method	2-bit ADPCM2 4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM	4-bit ADPCM 8-bit PCM	8-bit PCM 8-bit non-linear PCM	4-bit ADPCM 8-bit PCM 8-bit non-linear PCM
Max. number of phrases	256	127	63	247
Sampling frequency (kHz)	4.0/5.3/6.0/6.4/8.0/10.7 /12.0/12.8/16.0/21.3/ 24.0/25.6/32.0/42.7/ 48.0	4.0/5.3/6.4/8.0/ 10.7/12.8/16.0/ 32.0	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0
Clock frequency	4.096 MHz	256 kHz (CR oscillation) 4.096 MHz (XT)	256 kHz (CR oscillation) 4.096 MHz (XT)	4.096 MHz
D/A converter	Voltage type: 14 bits	Voltage type: 12 bits	Current type: 10 bits	Current type: 12 bits
Low-pass filter	FIR type interpolation filter	Secondary comb filter	Primary comb filter	Secondary comb filter
Number of channels	2 channels	2 channels	1 channel	1 channel
Phrase control table	Both 2 channels without user definable phrase restrictions	Can edit 8 phrases (1 channel only)	Can edit 8 phrases	None
Volume adjustment	29 steps (–2 dB/–5 dB steps)	4 steps (–6 dB steps)	Set at VREF.	Set at VREF.
Repeat function	No limit	4 types	None	None
STOP	Each channel independent	Simultaneous channels 1 and 2	Available	Available
Seam silence interval in continuous playback	0 (Note)	4 sampling cycles	3 sampling cycles	4 sampling cycles
Others	External data input possible	—	—	—

Note: Continuous playback shown in the figure below is possible.



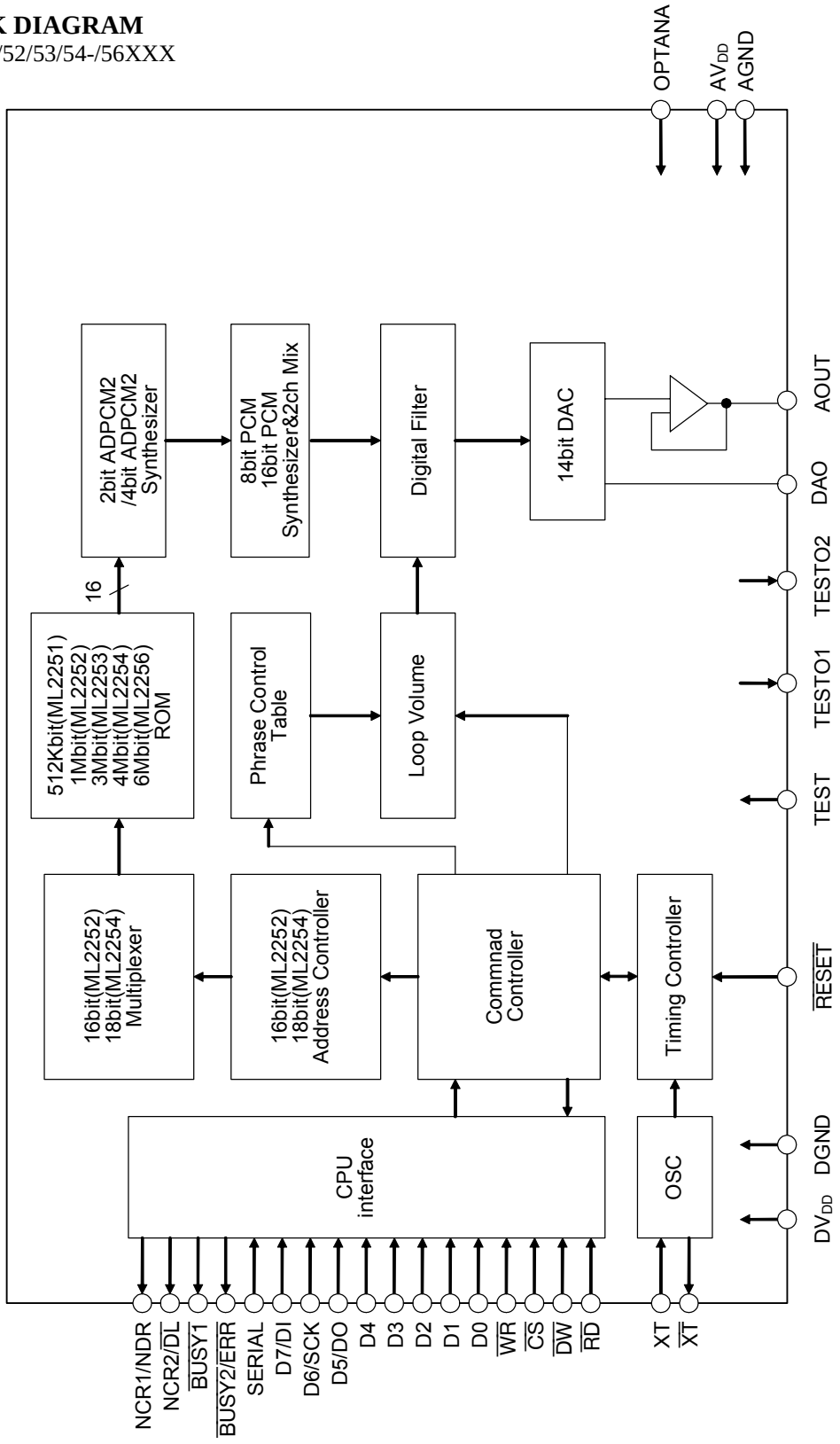
FEATURES

Type	ROM capacity	Maximum playback time length (sec) (In 4-bit ADPCM2)				
		F_{SAM} = 4.0 kHz	F_{SAM} = 6.4 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz	F_{SAM} = 32 kHz
ML2251	512 Kbit	31.7	19.8	15.8	7.9	3.9
ML2252	1 Mbit	64.5	40.3	32.2	16.1	8.0
ML2253	3 Mbit	195.5	122.2	97.7	48.8	24.4
ML2254	4 Mbit	261.1	163.2	130.5	65.2	32.6
ML22Q54	4 Mbit	261.1	163.2	130.5	65.2	32.6
ML2256	6 Mbit	392.1	245.1	196.0	98.0	49.0
ML22Q58	8 Mbit	522.2	326.4	261.0	130.4	65.2

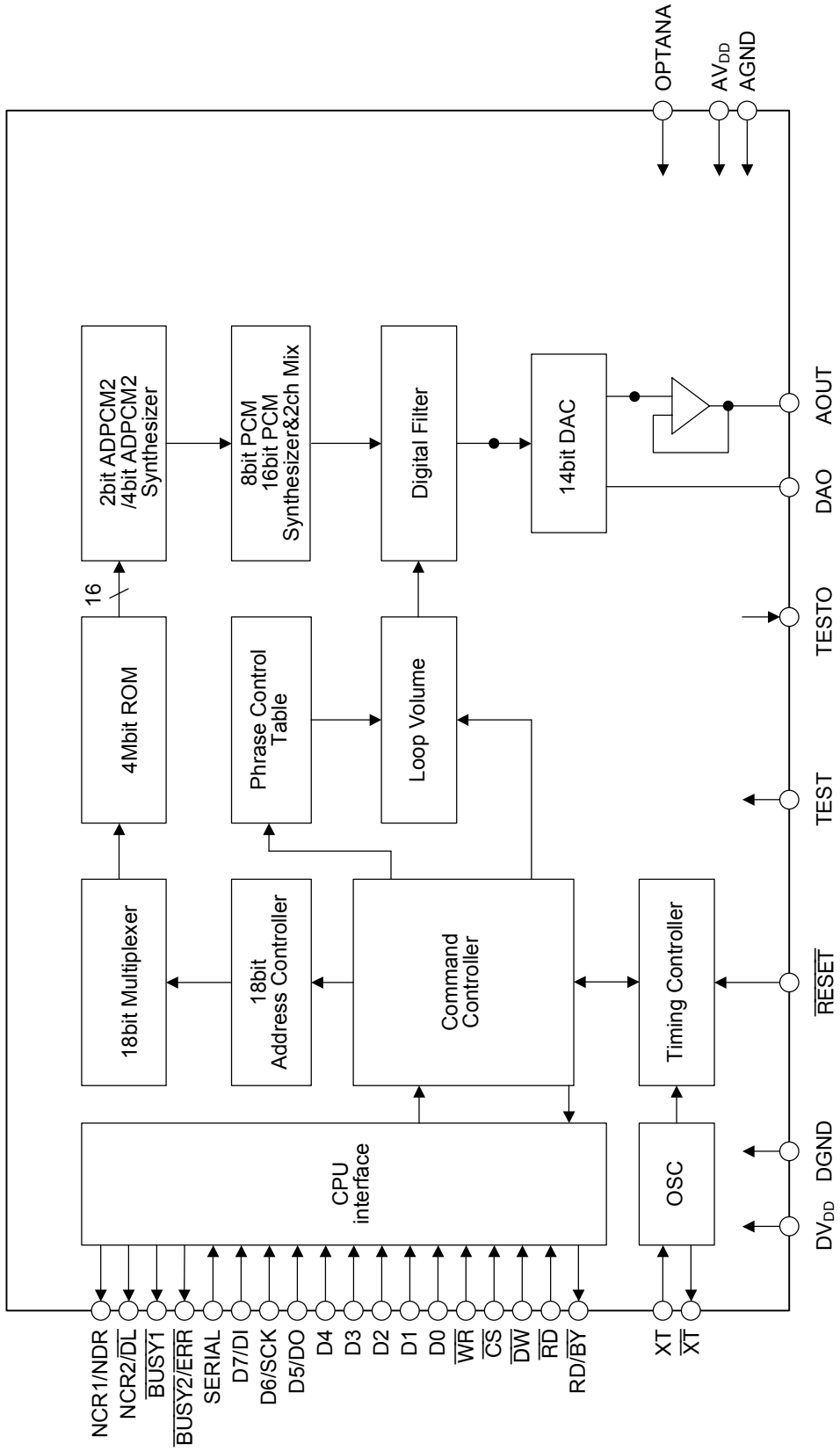
- Non-linear 8-bit PCM, 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms
- Serial input/parallel input selectable
- Phrase control table function i.e., user definable phrase control table function
- 2 channels mixing function
- Master clock frequency: 4.096 MHz
- Sampling frequency: 4.0 kHz, 5.3 kHz, 6.0kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.0kHz, 12.8 kHz, 16.0 kHz, 21.3 kHz, 24.0kHz, 25.6 kHz, 32.0 kHz, 42.7 kHz, 48 kHz
- Maximum number of phrases: 256 phrases
- Sound volume adjustment function built in (2 sounds independently adjustable in 29 steps)
- External voice data can be input
- 14-bit D/A converter built in
- Built-in low-pass filter: Digital filter
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K)
  (ML2251-XXXGA/ ML2252-XXXGA/ ML2253-XXXGA/ ML2254-XXXGA /ML2256-XXXGA / ML22Q54GA/ML22Q58GA)
  33-pin W-CSP (P-VFLGA33-5.03X5.78-0.80-W)
  (ML2253-XXXHB/ ML2254-XXXHB)

BLOCK DIAGRAM

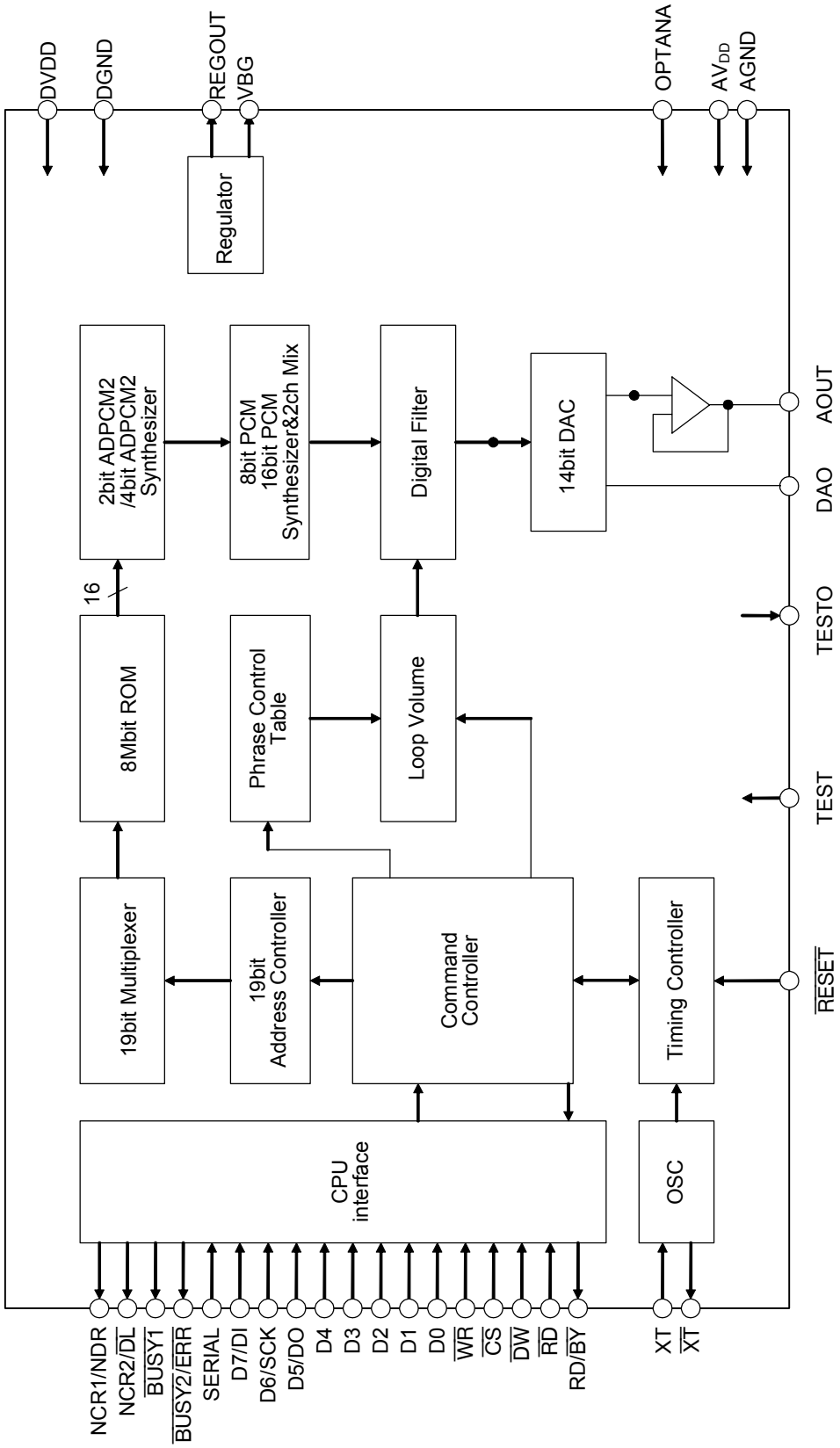
ML2251/52/53/54-/56XXX



ML22Q54


OPTANA
AVDD
AGND
2bit ADPCM2
/4bit ADPCM2
Synthesizer
8bit PCM
16bit PCM
Synthesizer&2ch Mix
Digital Filter
14bit DAC
AOUT
DAO
16
4Mbit ROM
Phrase Control
Table
Loop Volume
TESTO
TEST
18bit Multiplexer
18bit
Address Controller
Command
Controller
Timing Controller
RESET
CPU
interface
OSC
DGND
DVDD
NCR1/NDR
NCR2/DL
BUSY1
BUSY2/ERR
SERIAL
D7/DI
D6/SCK
D5/DO
D4
D3
D2
D1
D0
WR
CS
DW
RD
RD/BY
XT
XT

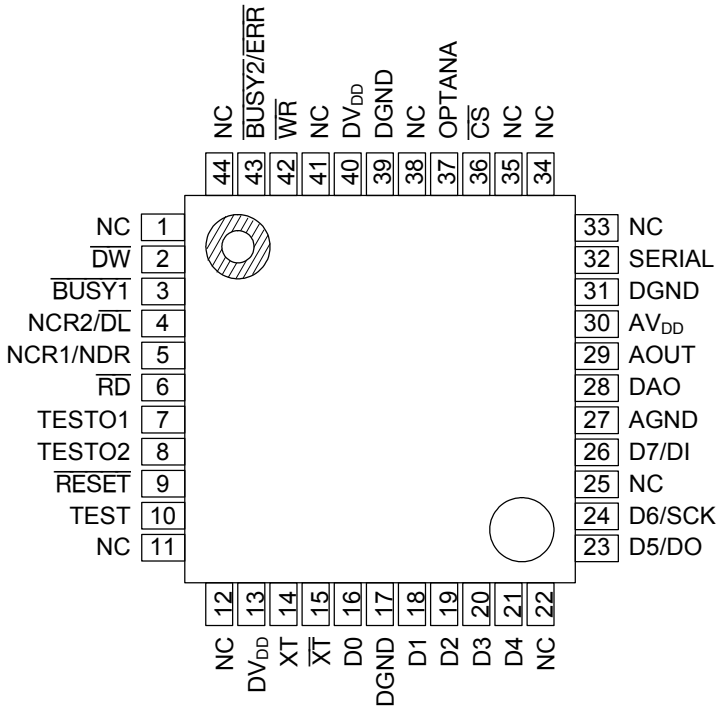
ML22Q58


DVDD
DGND
REGOUT
VBG
OPTANA
AVDD
AGND
Regulator
2bit ADPCM2 /4bit ADPCM2 Synthesizer
8bit PCM 16bit PCM Synthesizer&2ch Mix
Digital Filter
14bit DAC
AOUT
DAO
16
8Mbit ROM
Phrase Control Table
Loop Volume
TESTO
TEST
19bit Multiplexer
19bit Address Controller
Command Controller
Timing Controller
RESET
CPU interface
OSC
NCR1/NDR
NCR2/DL
BUSY1
BUSY2/ERR
SERIAL
D7/DI
D6/SCK
D5/DO
D4
D3
D2
D1
D0
WR
CS
DW
RD
RD/BY
XT
XT

PIN CONFIGURATION (TOP VIEW)

ML2251/52/53/54/56-XXXGA

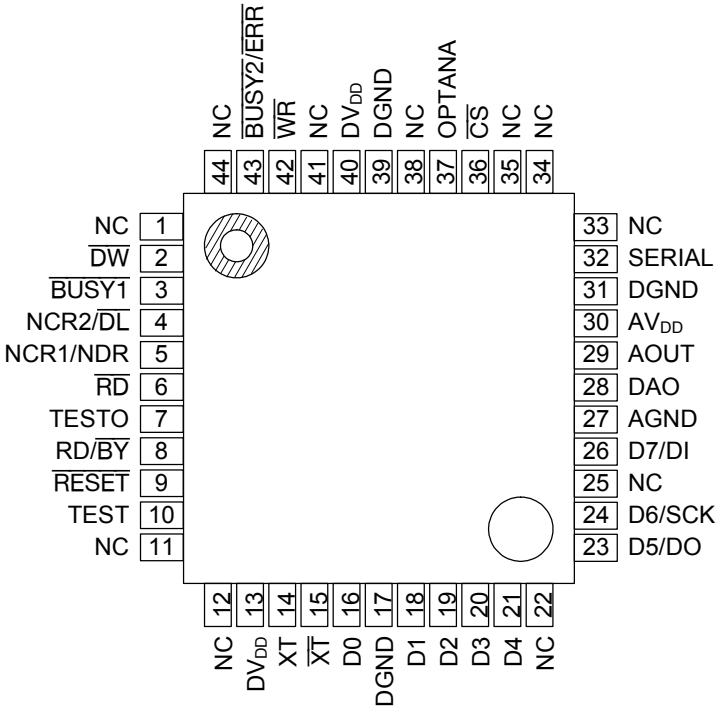
44-pin plastic QFP



NC: No Connection

ML22Q54GA

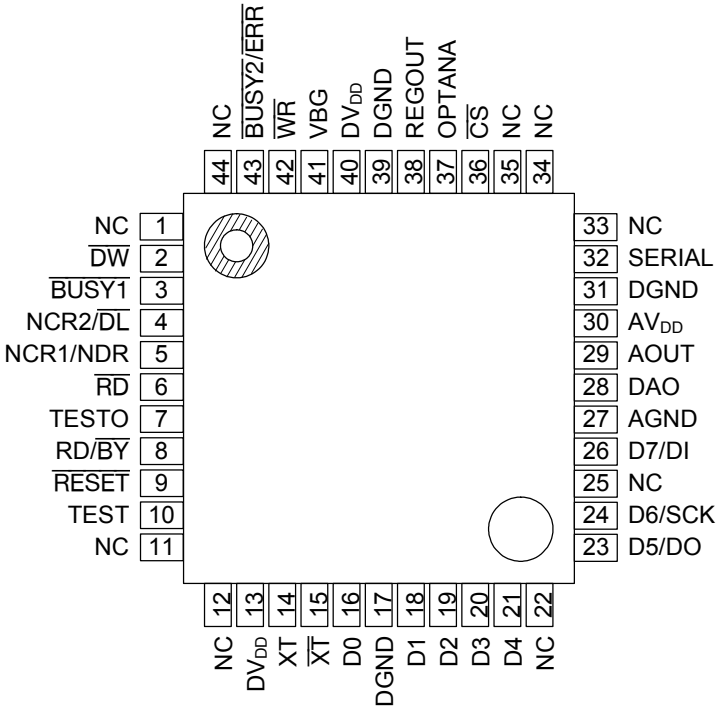
44-pin plastic QFP



NC: No Connection

ML22Q58GA

44-pin plastic QFP



NC: No Connection

ML2253/54-XXXHB

33pin W-CSP(Bottom View)

D5/DO	D3	D1	DGND	$\overline{XT}$	XT	6
D6/SCK	D4	D2	D0	DVDD	TEST	5
AGND			D7/DI	$\overline{RESET}$	TESTO2	4
DAO	AOUT		NCR1/NDR	TESTO1	$\overline{RD}$	3
AVDD	DGND	$\overline{CS}$	$\overline{WR}$	$\overline{BUSY1}$	NCR2/$\overline{DL}$	2
SERIAL	OPTANA	DGND	DVDD	$\overline{DW}$	$\overline{BUSY2/ERR}$	1
F	E	D	C	B	A	

PIN DESCRIPTIONS-1

ML2251/52/53/54/56-XXXGA and ML2253/54-XXXHB Common Pins

QFP Pin	WCSP pin	Symbol	Type	Description
43	A1	$\overline{\text{BUSY2}}/\overline{\text{ERR}}$	O	When using the built-in ROM for voice output, this pin outputs "L" level while channel 2 side processes a command and while plays back voice. Works as $\overline{\text{ERR}}$ pin when using the EXT command for voice output. If an abnormality occurred in the transfer of data, the pin will output "L" level and the voice output may become noisy. "H" level at power on.
3	B2	$\overline{\text{BUSY1}}$	O	Outputs "L" level while the channel 1 side processes a command and plays back voice. "H" level at power on.
4	A2	NCR2/$\overline{\text{DL}}$	O	The command input of channel 2 side is valid at "H" level when using the built-in ROM for voice output. Works as $\overline{\text{DL}}$ pin when using EXT command for the voice output. This pin outputs the signal that captures voice data to inside. The data is captured inside on the rising edge of $\overline{\text{DL}}$. "H" level at power on.
5	C3	NCR1/NDR	O	The command input of channel 1 side is valid at "H" level when using the built-in ROM for voice output. Works as NDR pin when using EXT command for the voice output. The voice data input is valid at "H" level. "H" level at power on.
9	B4	$\overline{\text{RESET}}$	I	At "L" level input, the device enters the initial state; the oscillation stops, and AOUT output and DAQ output are GND level at this time.
10	A5	TEST	I	Test pin for the device. Input "L" level to this pin. This pin has a pull-down resistor built in.
14	A6	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 15). When using an external clock, input the clock from this pin.
15	B6	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open.
16 18 19 20	E6 D5 D6 C5	D3 D2 D1 D0	I/O	CPU interface data bus pins in the parallel input interface. Channel status output pins at $\overline{\text{RD}}$ pin = "L" level. In the serial input interface, keep these pins at "L" level.
21	E5	D4	I/O	CPU interface data bus pin in the parallel input interface. When $\overline{\text{RD}}$ pin is at "L" level, this pin D4 usually outputs "L" level. In the serial input interface, keep this pin at "L" level.
23	F6	D5/DO	I/O	CPU interface data bus pin in the parallel input interface. When $\overline{\text{RD}}$ pin is at "L" level, this D5/DO pin usually outputs "L" level. Works as channel status output pin in the serial interface. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins are "L" level, the status of each channel is output serially from this D5/DO pin in synchronization with SCK clock.

QFP Pin	WCSP pin	Symbol	Type	Description
24	F5	D6/SCK	I/O	CPU interface data bus pin in the parallel input interface. Usually outputs “L” level when $\overline{RD}$ = “L” level. Works as serial clock input pin in the serial input interface. When the SCK input is at “L” level on the falling edge of $\overline{CS}$, the DI input is captured in the device on the rising edge of SCK clock. And when the SCK input is at “H” level on the falling edge of $\overline{CS}$, the DI input is captured on the falling edge of SCK clock.
26	C4	D7/DI	I/O	CPU interface data bus pin in the parallel input interface. Usually output “L” level when $\overline{RD}$ is at “L” level. Works as serial data input pin in the serial input interface.
28	F3	DAO	O	DAO pin outputs analog signal of 14-bit DAC.
29	E3	AOUT	O	AOUT pin usually outputs the analog signal of 14-bit DAC via voltage follower.
32	F1	SERIAL	I	CPU interface switching pin. Serial input interface at “H” level. And parallel input interface at “L” level.
36	D2	$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ pin is at “H” level, the $\overline{WR}$, $\overline{DW}$, and $\overline{RD}$ signals cannot be input to the device.
37	E1	OPTANA	I	Keep this pin “L” level. The analog signal of 14-bit DAC is output from DAO pin and from AOUT pin via voltage follower.
42	C2	$\overline{WR}$	I	CPU interface write signal. When $\overline{CS}$ pin is at “H” level, the $\overline{WR}$ signal cannot be input to the device.
2	B1	$\overline{DW}$	I	Data write signal when using EXT command for the voice output. Set the pin to “H” level when not using EXT command. When $\overline{CS}$ pin is at “H” level, the $\overline{DW}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
6	A3	$\overline{RD}$	I	CPU interface read signal. When $\overline{CS}$ pin is at “H” level, the $\overline{RD}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
7, 8	B3, A4	TESTO1 TESTO2	O	Output pin for testing. Keep this pin open.
30	F2	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
13, 40	B5, C1	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
27	F4	AGND	—	Analog ground pin.
17, 31, 39	C6, D1, E2	DGND	—	Digital ground pin.

PIN DESCRIPTIONS-2

ML22Q54/Q58GA Common Pins
44-pin plastic QFP

Pin	Symbol	Type	Description
43	$\overline{\text{BUSY2}}/\overline{\text{ERR}}$	O	When using the built-in ROM for voice output, this pin outputs "L" level while channel 2 side processes a command and while plays back voice. Works as $\overline{\text{ERR}}$ pin when using EXT command for the voice output. If an abnormality occurred in the transfer of data, the $\overline{\text{ERR}}$ pin outputs "L" level and the voice output may become noisy. "H" level at power on.
3	$\overline{\text{BUSY1}}$	O	Outputs "L" level while the channel 1 side processes a command and while plays back voice. "H" level at power on.
4	NCR2/$\overline{\text{DL}}$	O	The input command of channel 2 is valid at "H" level when using the built-in ROM for voice output. $\overline{\text{DL}}$ pin when using EXT command for the voice output. It outputs the voice data capture signal. The data is captured on the rising edge of $\overline{\text{DL}}$. "H" level at power on.
5	NCR1/NDR	O	The command input of channel 1 side is valid at "H" level when using the built-in ROM for voice output. NDR pin when using EXT command for the voice output. The voice data input is effective at "H" level. "H" level at power on.
9	$\overline{\text{RESET}}$	I	When "L" level is input to this pin, the device is reset, the oscillation stops, and AOUT and DAQ outputs go into GND level.
10	TEST	I	Test pin for the device. Input "L" level to this pin. This pin has a pull-down resistor built in.
14	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 15). When using an external clock, input the clock from this pin.
15	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open.
16 18 19 20	D3 D2 D1 D0	I/O	CPU interface data bus pins in the parallel input interface. Channel status output pins when $\overline{\text{RD}}$ is at "L" level. The pins output the flash memory data when reading the built-in flash memory data. In the serial input interface, keep these pins at "L" level.
21	D4	I/O	CPU interface data bus pin in the parallel input interface. The pin outputs flash memory data when reading the built-in flash memory data. When $\overline{\text{RD}}$ is at "L" level other than when reading the flash memory data, this pin usually outputs "L" level. In the serial input interface, keep this pin at "L" level.
23	D5/DO	I/O	CPU interface data bus pin in the parallel input interface. The pin outputs flash memory data when reading the built-in flash memory data. When $\overline{\text{RD}}$ is at "L" level other than when reading the flash memory data, this pin usually outputs "L" level. Channel status output pin in the serial input interface. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are at "L" level, this D5/DO pin serially outputs the status of each channel in synchronization with SCK clock. When reading data of the built-in flash memory, the pin will output serially the flash memory data.

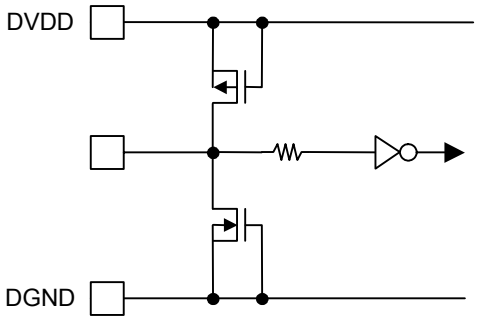
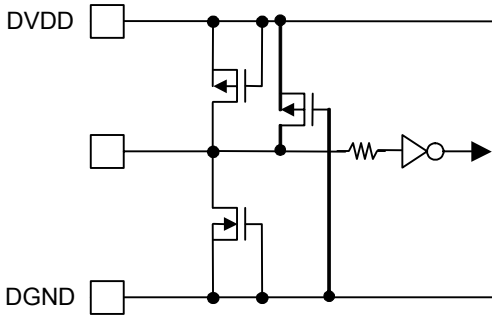
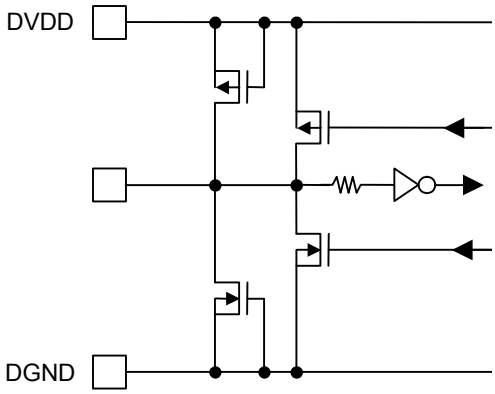
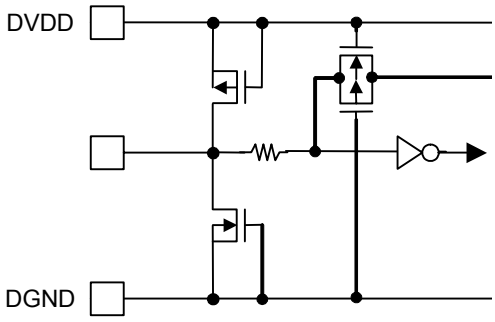
Pin	Symbol	Type	Description
24	D6/SCK	I/O	Works as CPU interface data bus pin in parallel input interface. Works as flash memory data output pin when reading the built-in flash memory data. When $\overline{RD}$ is at "L" level other than when reading the flash memory data, this D6/SCK pin usually outputs "L" level. Works as serial clock input pin in the serial input interface. When the SCK input is at "L" level on the falling edge of $\overline{CS}$, the DI input is captured in device on the rising edge of SCK clock. And when the SCK input is at "H" level on the falling edge of $\overline{CS}$, the DI input is captured on the falling edge of SCK clock.
26	D7/DI	I/O	Works as CPU interface data bus pin in the parallel input interface. Works as flash data output pin when reading the built-in flash memory data. When $\overline{RD}$ is at "L" level at times other than reading the flash memory data, this D7/DI pin usually outputs "L" level. Works as serial data input pin in the serial input interface.
28	DAO	O	DAO pin outputs the 14-bit DAC analog signal.
29	AOUT	O	AOUT pin outputs the 14-bit DAC analog signal via voltage follower.
32	SERIAL	I	CPU interface switching pin. At "H" level: Serial input interface. At "L" level: Parallel input interface.
36	$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$, $\overline{DW}$, and $\overline{RD}$ signals cannot be input to the device.
37	OPTANA	I	Keep this pin "L" level. 14-bit DAC analog signal is output from DAO pin and 14-bit DAC analog signal is output from AOUT pin via the voltage follower.
42	$\overline{WR}$	I	CPU interface write signal. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$ signal cannot be input to the device.
2	$\overline{DW}$	I	Data write signal at EXT command and Flash I/F command. When the EXT and Flash I/F commands are not used, keep this pin at "H" level. When $\overline{CS}$ pin is at "H" level, the $\overline{DW}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
6	$\overline{RD}$	I	CPU interface read signal. This pin is used when reading the status signal of each channel or when reading data of the built-in flash memory. When not in use, keep this pin to "H" level. This pin has a pull-up resistor built in.
7	TESTO	O	Output pin for testing. Keep this pin open.
8	RD/BY	O	Output pin to indicate the automatic erase/write status of the built-in flash memory. Outputs "L" level during erase or programming cycle to indicate the busy state. Goes to "H" level at the end of the erase or programming cycle and enters into the ready state.

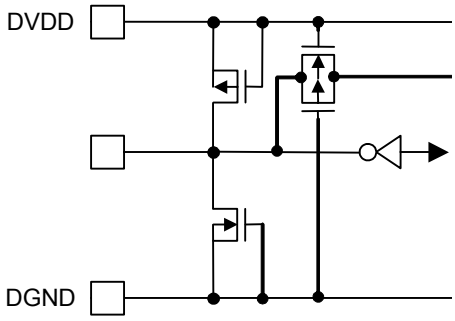
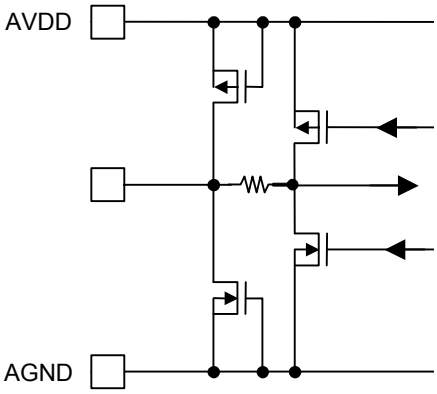
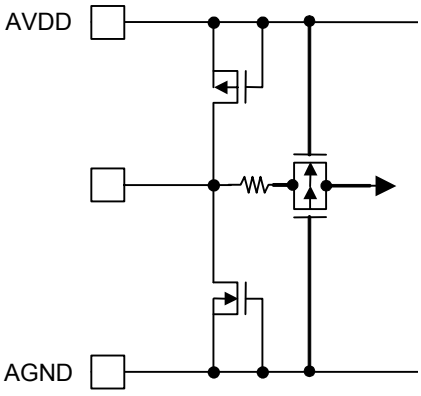
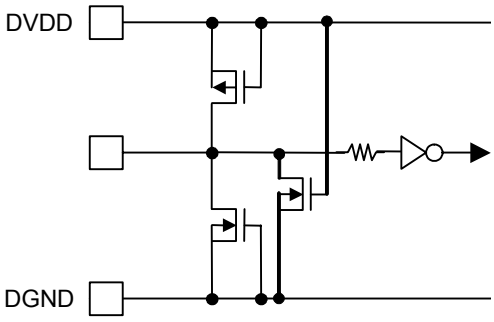
Pin	Symbol	Type	Description
30	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
13, 40	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
27	AGND	—	Analog ground pin.
17, 31, 39	DGND	—	Digital ground pin.

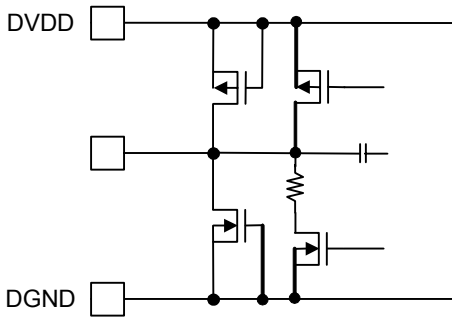
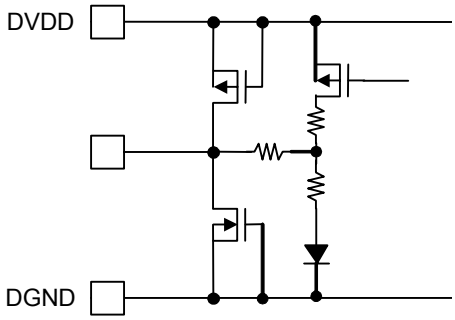
Applicable to ML22Q58 Pins

Pin	Symbol	Type	Description
38	REGOUT	O	3V regulator output pin for the built-in flash power supplies. Connect a 10μF or larger condenser between REGOUT pin and DGND pin.
41	VBG	O	Reference voltage output pin for regulator. Recommends connecting a 150pF condenser between REGOUT pin and DGND pin.

PIN EQUIVALENT CIRCUITS

Symbol	Equivalent Circuit
RESET CS WR OPTANA	
RD DW	
SERIAL D7-D0 BUSY1 BUSY2 NCR1 NCR2	
XT	

Symbol	Equivalent Circuit
XT	
AOUT	
DAO	
TEST	

Symbol	Equivalent Circuit
REGOUT (Applies to ML22Q58)	
VBG (Applies to ML22Q58)	

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C ML2251/52/53/54/56-XXX ML22Q58	–0.3 to +7.0	V
		Ta = 25°C, ML22Q54	–0.3 to +4.6	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} +0.3	V
Power Dissipation	P_D	Ta = 25°C	900	mW
Output short current	I_{SC}	Ta = 25°C, Applies to output pins excluding REGOUT pin	6	mA
		Ta = 25°C, Applies to REGOUT pin	45	mA
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (3 V)

ML225152/53/54/56-XXX, ML22Q54/Q58

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	ML2251/52/53/54/56-XXX, ML22Q54	2.7 to 3.6			V
		ML22Q58	2.7 to 3.3			V
Operating temperature	T_{OP}	ML2251/52/53/54/56-XXX	–40 to +85			°C
		ML22Q54/Q58	0 to +70			
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

RECOMMENDED OPERATING CONDITIONS (5 V)

ML2251/52/53/54/56-XXX, ML22Q58

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	—	4.5 to 5.5			V
Operating temperature	T_{OP}	ML2251/52/53/54/56-XXX	–40 to +85			°C
		ML22Q58	0 to +70			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

ML2251/52/53/54/56-XXX, ML22Q54/Q58

ML2251/52/53/54/56-XXX: $DV_{DD} = AV_{DD}$ = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: $DV_{DD} = AV_{DD}$ = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C
ML22Q58 : $DV_{DD} = AV_{DD}$ = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.14 × V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	μA
"H" input current 2 (Note 1)	I_{IH2}	$V_{IH} = V_{DD}$	0.3	2.0	15	μA
"H" input current 3 (Note 2)	I_{IH3}	$V_{IH} = V_{DD}$ Pull-down resistor built in pin	8	40	130	μA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	μA
"L" input current 2 (Note 3)	I_{IL2}	V_{IL} = GND Pull-up resistor built in pin	–120	–40	–10	μA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–15	–2.0	–0.3	μA
Playback Operating current consumption	I_{DD1}	f_{OSC} = 4.096 MHz at no load (ML2251/52/53/54/56-XXX)	—	6	35	mA
	I_{DD2}	f_{OSC} = 4.096 MHz at no load (ML22Q54/Q58)	—	9	35	mA
Built-in Flash memory access Operating current consumption 1	I_{DD3}	f_{OSC} = 4.096 MHz at no load Read Operation (ML22Q54/Q58)	—	10	35	mA
Built-in Flash memory access Operating current consumption 2	I_{DD4}	f_{OSC} = 4.096 MHz at no load Write and Erase Operation (ML22Q54/Q58)	—	20	60	mA
Standby current consumption	I_{DDS}	Ta = –40 to +70°C	—	—	15	μA
		Ta = –40 to +85°C	—	—	50	μA
		Ta = 0 to +70°C (ML22Q54/Q58)	—	—	55	μA

Notes: 1. Applies to XT pin.
2. Applies to TEST pin.
3. Applies to $\overline{RD}$ and $\overline{DW}$ pins.

DC Characteristics (5 V)

ML2251/52/53/54/56-XXX, ML22Q58

ML2251/52/53/54/56-XXX : DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.2 × V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	μA
"H" input current 2 (Note 1)	I_{IH2}	V_{IH} = V_{DD}	0.8	5.0	20	μA
"H" input current 3 (Note 2)	I_{IH3}	V_{IH} = V_{DD} Pull-down resistor built in pin	30	—	350	μA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	μA
"L" input current 2 (Note 3)	I_{IL2}	V_{IL} = GND Pull-up resistor built in pin	–230	—	–60	μA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–20	–5.0	–0.8	μA
Operating current consumption	I_{DD1}	f_{OSC} = 4.096 MHz at no load (ML2251/52/53/54/56-XXX)	—	19	40	mA
	I_{DD2}	f_{OSC} = 4.096 MHz at no load (ML22Q58)	—	22	40	mA
Built-in Flash memory access Operating current consumption 1	I_{DD3}	f_{OSC} = 4.096 MHz at no load Read Operation (ML22Q58)	—	23	40	mA
Built-in Flash memory access Operating current consumption 2	I_{DD4}	f_{OSC} = 4.096 MHz at no load Write and Erase Operation (ML22Q58)	—	33	60	mA
Standby current consumption	I_{DDS}	Ta = –40 to +70°C	—	—	15	μA
		Ta = –40 to +85°C	—	—	100	μA
		Ta = 0 to +70°C (ML22Q58)	—	—	100	μA

Notes: 1. Applies to XT pin.
2. Applies to TEST pin.
3. Applies to $\overline{RD}$ and $\overline{DW}$ pins.

Analog Section Characteristics (3 V)
ML2251/52/53/54/56-XXX, ML22Q54/Q58

ML2251/52/53/54/56-XXX: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} –0.5	V
DAO output impedance	R_{DAO}	—	30	50	70	kΩ

Analog Section Characteristics (5 V)
ML2251/52/53/54/56-XXX, ML22Q58

ML2251/52/53/54/56-XXX : DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} –0.5	V
DAO output impedance	R_{DAO}	—	30	50	70	kΩ
REGOUT output voltage	V_{REGO}	ML22Q58	2.7	3	3.3	V
VBG output voltage	V_{BG}	ML22Q58	1.0	1.3	1.5	V

AC Characteristics (3 V)
ML2251/52/53/54/56-XXX, ML22Q54/Q58

ML2251/52/53/54-XXX: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	t_{RST}	—	1	—	—	μs
$\overline{CS}$ setup time for falling edge of $\overline{WR}$	t_{CWS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{WR}$	t_{CWH}	—	30	—	—	ns
$\overline{WR}$ pulse width	t_{WR}	SERIAL pin = “L”	200	—	—	ns
Data setup time for rising edge of $\overline{WR}$	t_{DIS1}	SERIAL pin = “L”	100	—	—	ns
Data hold time for rising edge of $\overline{WR}$	t_{DIH1}	SERIAL pin = “L”	30	—	—	ns
$\overline{CS}$ setup time for falling edge of $\overline{RD}$	t_{CRS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{RD}$	t_{CRH}	—	0	—	—	ns
$\overline{RD}$ pulse width 1	t_{RD}	Status Read	200	—	—	ns
$\overline{RD}$ pulse width 2	t_{RD}	Data Read	300	—	—	ns
Data output delay time 1 for falling edge of $\overline{RD}$	t_{DOD1}	Status Read	—	—	100	ns
Data output delay time 2 for falling edge of $\overline{RD}$	t_{DOD3}	Data Read	—	—	200	ns
Data output hold time 1 for rising edge of $\overline{RD}$	t_{DOH1}	R_L=3kΩ	—	—	100	ns
SCK setup time for falling edge of $\overline{CS}$	t_{CKS}	SERIAL pin = “H”	200	—	—	ns
SCK hold time for falling edge of $\overline{CS}$	t_{CKH}	SERIAL pin = “H”	200	—	—	ns
Data setup time for rising edge of SCK	t_{DIS2}	SERIAL pin = “H”	30	—	—	ns
Data hold time for rising edge of SCK	t_{DIH2}	SERIAL pin = “H”	30	—	—	ns
SCK “H” level pulse width	t_{SCKH}	SERIAL pin = “H”	200	—	—	ns
SCK “L” level pulse width	t_{SCKL}	SERIAL pin = “H”	200	—	—	ns
$\overline{WR}$ hold time for rising edge of SCK	t_{SWH}	SERIAL pin = “H”	200	—	—	ns
Data output enable time for falling edge of RD	t_{DOE}	SERIAL pin = “H”	—	—	100	ns
Data output delay time for rising edge of SCK	t_{DOD2}	SERIAL pin = “H”	—	—	100	ns
Data output hold time 2 for rising edge of $\overline{RD}$	t_{DOH2}	SERIAL pin = “H” R_L=3kΩ	—	—	100	ns
Interval time 1 from rising edge of $\overline{CS}$ up to the next falling edge of $\overline{CS}$	t_{INTW}	STOP, LOOP, VOL, EXT, and FLASH command input f_{OSC} = 4.096 MHz	1.3	—	—	μs
Interval time 2 from rising edge of $\overline{CS}$ up to the next falling edge of $\overline{CS}$	t_{INTR}	Data read	200	—	—	ns
NCRn output delay time for rising edge of $\overline{WR}$	t_{NCRD}	—	—	—	100	ns
$\overline{BUSY}$n output delay time for rising edge of $\overline{WR}$	t_{BSYD}	—	—	—	100	ns
“L” level output time of NCRn and $\overline{BUSY}$n at PUP1 command input	t_{PUP1}	f_{OSC} = 4.096 MHz	1.9	2	2.1	ms
Oscillation stabilized time at PUP1 and PUP2 commands input	t_{OSC}	f_{OSC} = 4.096 MHz	1.9	2	2.1	ms
“L” level output time of NCRn and $\overline{BUSY}$n at PUP2 command input	t_{PUP2}	f_{OSC} = 4.096 MHz	65	66	67	ms
Analog output ramp-up time at PUP2 command input	t_{AUP}	f_{OSC} = 4.096 MHz	63	64	65	ms

ML2251/52/53/54/56-XXX: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" level output time of NCRn and $\overline{BUSYn}$ at PDWN1 command input	t_{PD1}	f_{OSC} = 4.096 MHz	0.4	—	1.3	µs
"L" level output time of NCRn and $\overline{BUSYn}$ at PDWN2 command input	t_{PD2}	f_{OSC} = 4.096 MHz	63	64	65	ms
Command processing time at PDWN2 command input	t_{AD}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
Analog output ramp-down time at PDWN2 command input	t_{ADWN}	f_{OSC} = 4.096 MHz	63	64	65	ms
NCRn "L" level output time 1	t_{NCR1}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
NCRn "L" level output time 2 (Note 1)	t_{NCR2}	f_{OSC} = 4.096 MHz Phrase sampling frequency of previous playback = 4kHz	3.88	4.125	4.38	ms
NCRn "L" level output time 3 (Note 1)	t_{NCR3}		3.88	4.125	4.38	ms
$\overline{BUSYn}$ "L" level output time	t_{BSY1}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
Interval time from rising edge of NCRn up to the next falling edge of $\overline{CS}$	t_{NCS}	Command Input	30	—	—	ns
Interval time from rising edge of $\overline{BUSYn}$ up to the next falling edge of $\overline{CS}$	t_{BCS}	Command Input	30	—	—	ns
"L" level output time of NCRn at CLOOP command input	t_{LPC}	f_{OSC} = 4.096 MHz	0.2	—	17769	µs
$\overline{CS}$ setup time for falling edge of $\overline{DW}$	t_{CDS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{DW}$	t_{CDH}	—	30	—	—	ns
$\overline{DW}$ pulse width	t_{WD}	SERIAL pin = "L"	200	—	—	ns
Data setup time for rising edge of $\overline{DW}$	t_{DIS3}	SERIAL pin = "L"	100	—	—	µs
Data hold time for rising edge of $\overline{DW}$	t_{DIH3}	SERIAL pin = "L"	30	—	—	ns
"L" level output time of NCRn and $\overline{BUSYn}$ at EXT command input	t_{EXT}	f_{OSC} = 4.096 MHz	0.2	—	260	µs
NDR output delay time for rising edge of $\overline{DW}$	t_{NDRD}	—	—	—	100	ns
$\overline{DL}$ "L" level pulse width 1	t_{WDL1}	f_{OSC} = 4.096 MHz	5.68	5.86	6.04	µs
$\overline{DL}$ "L" level pulse width 2 (Note 2)	t_{WDL2}	f_{OSC} = 4.096 MHz Sampling frequency = 32 kHz	5.68	5.86	6.04	µs
$\overline{DL}$ "H" level pulse width 1	t_{WDH1}	f_{OSC} = 4.096 MHz	128	133	137	µs
$\overline{DL}$ "H" level pulse width 2	t_{WDH2}	f_{OSC} = 4.096 MHz	106	112	116	µs
$\overline{DL}$ pulse period (Note 1)	t_{PDL}	f_{OSC} = 4.096 MHz 8-bit linear/non-linear PCM, 16-bit linear PCM algorithm Sampling frequency = 4 kHz	242	250	258	µs
		f_{OSC} = 4.096 MHz 4-bit ADPCM 2 Sampling frequency = 4 kHz	484	500	516	µs
		f_{OSC} = 4.096 MHz 2-bit ADPCM 2 Sampling frequency = 4 kHz	0.97	1.00	1.03	ms
NDR "L" level pulse width when 16-bit PCM upper 8-bit data is input.	t_{WNL}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs

Note: Proportional to a sampling frequency.
Note: Proportional to the frequency of a sampling frequency group. 32kHz group expresses one of 32kHz/16kHz/8kHz/4kHz.

Applicable to ML22Q54

$DV_{DD} = AV_{DD}$ = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFW}	f_{OSC} = 4.096 MHz	—	—	30	μs
"L" level pulse width of RD/$\overline{BY}$ to write data to flash memory	t_{FW}	f_{OSC} = 4.096 MHz	—	—	25	μs
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFE}	f_{OSC} = 4.096 MHz	—	—	25.1	ms
"L" level pulse width of RD/BY to erase data from flash memory	t_{FE}	f_{OSC} = 4.096 MHz	—	—	25	ms

Applicable to ML22Q58

$DV_{DD} = AV_{DD}$ = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFW}	f_{OSC} = 4.096 MHz	—	—	105	μs
"L" level pulse width of RD/$\overline{BY}$ to write data to flash memory	t_{FW}	f_{OSC} = 4.096 MHz	—	—	100	μs
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFE}	f_{OSC} = 4.096 MHz	—	—	3	Sec
"L" level pulse width of RD/BY to erase data from flash memory	t_{FE}	f_{OSC} = 4.096 MHz	—	—	3	sec

AC Characteristics (5 V)
ML2251/52/53/54/56-XXX, ML22Q58

ML2251/52/53/54/56-XXX: DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	t_{RST}	—	1	—	—	μs
$\overline{CS}$ setup time for falling edge of $\overline{WR}$	t_{CWS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{WR}$	t_{CWH}	—	30	—	—	ns
$\overline{WR}$ pulse width	t_{WR}	SERIAL pin = “L”	200	—	—	ns
Data setup time for rising edge of $\overline{WR}$	t_{DIS1}	SERIAL pin = “L”	100	—	—	ns
Data hold time for rising edge of $\overline{WR}$	t_{DIH1}	SERIAL pin = “L”	30	—	—	ns
$\overline{CS}$ setup time for falling edge of $\overline{RD}$	t_{CRS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{RD}$	t_{CRH}	—	0	—	—	ns
$\overline{RD}$ pulse width	t_{RD}	—	200	—	—	ns
Data output delay time for falling edge of $\overline{RD}$	t_{DOD1}	—	—	—	100	ns
Data output hold time 1 for rising edge of $\overline{RD}$	t_{DOH1}	R_L=3kΩ	—	—	100	ns
SCK setup time for falling edge of $\overline{CS}$	t_{CKS}	SERIAL pin = “H”	200	—	—	ns
SCK hold time for falling edge of $\overline{CS}$	t_{CKH}	SERIAL pin = “H”	200	—	—	ns
Data setup time for rising edge of SCK	t_{DIS2}	SERIAL pin = “H”	30	—	—	ns
Data hold time for rising edge of SCK	t_{DIH2}	SERIAL pin = “H”	30	—	—	ns
SCK “H” level pulse width	t_{SCKH}	SERIAL pin = “H”	200	—	—	ns
SCK “L” level pulse width	t_{SCKL}	SERIAL pin = “H”	200	—	—	ns
$\overline{WR}$ hold time for rising edge of SCK	t_{SWH}	SERIAL pin = “H”	200	—	—	ns
Data output enable time for falling edge of $\overline{RD}$	t_{DOE}	SERIAL pin = “H”	—	—	100	ns
Data output delay time for rising edge of SCK	t_{DOD2}	SERIAL pin = “H”	—	—	100	ns
Data output hold time 2 for rising edge of $\overline{RD}$	t_{DOH2}	SERIAL pin = “H” R_L=3kΩ	—	—	100	ns
Interval time 1 from rising edge of $\overline{CS}$ up to the next falling edge of $\overline{CS}$	t_{INTW}	STOP, LOOP, VOL, and EXT commands input f_{OSC} = 4.096 MHz	1.3	—	—	μs
Interval time 2 from rising edge of $\overline{CS}$ up to the next falling edge of $\overline{CS}$	t_{INTR}	Data read	200	—	—	ns
NCRn output delay time for rising edge of $\overline{WR}$	t_{NCRD}	—	—	—	100	ns
$\overline{BUSYn}$ output delay time for rising edge of $\overline{WR}$	t_{BSYD}	—	—	—	100	ns
“L” level output time of NCRn and $\overline{BUSYn}$ at PUP1 command input	t_{PUP1}	f_{OSC} = 4.096 MHz	1.9	2	2.1	ms
Oscillation stabilization time at PUP1 and PUP2 commands input	t_{OSC}	f_{OSC} = 4.096 MHz	1.9	2	2.1	ms
“L” level output time of NCRn and $\overline{BUSYn}$ at PUP2 command input	t_{PUP2}	f_{OSC} = 4.096 MHz	65	66	67	ms

ML2251/52/53/54/56-XXX: DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q58 : DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog output ramp-up time at PUP2 command input	t_{AUP}	f_{OSC} = 4.096 MHz	63	64	65	ms
"L" level output time of NCRn and $\overline{BUSYn}$ at PDWN1 command input	t_{PD1}	f_{OSC} = 4.096 MHz	0.4	—	1.3	µs
"L" level output time of NCRn and $\overline{BUSYn}$ at PDWN2 command input	t_{PD2}	f_{OSC} = 4.096 MHz	63	64	65	ms
Command processing time at PDWN2 command input	t_{AD}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
Analog output ramp-down time at PDWN2 command input	t_{ADWN}	f_{OSC} = 4.096 MHz	63	64	65	ms
NCRn "L" level output time 1	t_{NCR1}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
NCRn "L" level output time 2 (Note 1)	t_{NCR2}	f_{OSC} = 4.096 MHz Phrase sampling frequency of previous playback = 4kHz group	3.88	4.125	4.38	ms
NCRn "L" level output time 3 (Note 1)	t_{NCR3}		3.88	4.125	4.38	ms
$\overline{BUSYn}$ "L" level output time	t_{BSY1}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs
Interval time from rising edge of NCRn up to the next falling edge of $\overline{CS}$	t_{NCS}	Command Input	30	—	—	ns
Interval time from rising edge of $\overline{BUSYn}$ up to the next falling edge of $\overline{CS}$	t_{BCS}	Command Input	30	—	—	ns
"L" level output time of NCRn at CLOOP command input	t_{LPC}	f_{OSC} = 4.096 MHz	0.2	—	17769	µs
$\overline{CS}$ setup time for falling edge of $\overline{DW}$	t_{CDS}	—	0	—	—	ns
$\overline{CS}$ hold time for rising edge of $\overline{DW}$	t_{CDH}	—	30	—	—	ns
$\overline{DW}$ pulse width	t_{WD}	SERIAL pin = "L"	200	—	—	ns
Data setup time for rising edge of $\overline{DW}$	t_{DIS3}	SERIAL pin = "L"	100	—	—	µs
Data hold time for rising edge of $\overline{DW}$	t_{DIH3}	SERIAL pin = "L"	30	—	—	ns
"L" level output time of NCRn and $\overline{BUSYn}$ at EXT command input	t_{EXT}	f_{OSC} = 4.096 MHz	0.2	—	260	µs
NDR output delay time for rising edge of $\overline{DW}$	t_{NDRD}	—	—	—	100	ns
$\overline{DL}$ "L" level pulse width 1	t_{WDL1}	f_{OSC} = 4.096 MHz	5.68	5.86	6.04	µs
$\overline{DL}$ "L" level pulse width 2 (Note 2)	t_{WDL2}	f_{OSC} = 4.096 MHz Sampling frequency = 32 kHz group	5.68	5.86	6.04	µs
$\overline{DL}$ "H" level pulse width 1	t_{WDH1}	f_{OSC} = 4.096 MHz	128	133	137	µs
$\overline{DL}$ "H" level pulse width 2	t_{WDH2}	f_{OSC} = 4.096 MHz	106	112	116	µs
$\overline{DL}$ pulse period (Note 1)	t_{PDL}	f_{OSC} = 4.096 MHz 8-bit linear/non-linear PCM, 16-bit linear PCM Sampling frequency = 4 kHz	242	250	258	µs
		f_{OSC} = 4.096 MHz 4-bit ADPCM 2 Sampling frequency = 4 kHz	484	500	516	µs
		f_{OSC} = 4.096 MHz 2-bit ADPCM 2 Sampling frequency = 4 kHz	0.97	1.00	1.03	ms
NDR "L" level pulse width when 16-bit high order 8-bit data is input.	t_{WNL}	f_{OSC} = 4.096 MHz	0.5	—	1.4	µs

Applicable to ML22Q58

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = 0 to +70°C

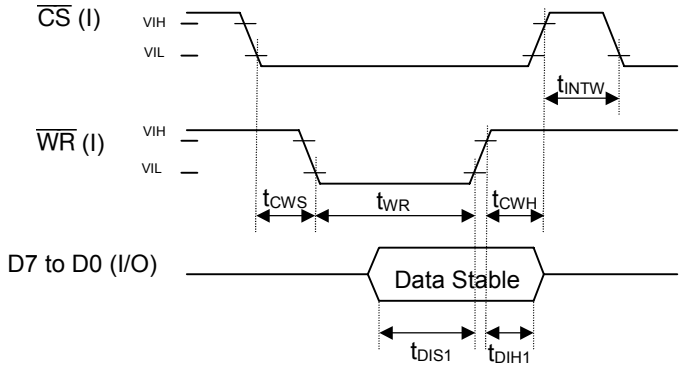
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFW}	f_{OSC} = 4.096 MHz	–	–	105	μs
"L" level pulse width of RD/$\overline{BY}$ to write data to flash memory	t_{FW}	f_{OSC} = 4.096 MHz	–	–	100	μs
"L" level pulse width of NCRn and $\overline{BUSYn}$ to write data to flash memory	t_{WFE}	f_{OSC} = 4.096 MHz	–	–	3	Sec
"L" level pulse width of RD/BY to erase data from flash memory	t_{FE}	f_{OSC} = 4.096 MHz	–	–	3	sec

Note: Proportional to a sampling frequency.
Note: Proportional to the frequency of a sampling frequency group. 32kHz group expresses one of 32kHz/16kHz/ 8kHz/4kHz.

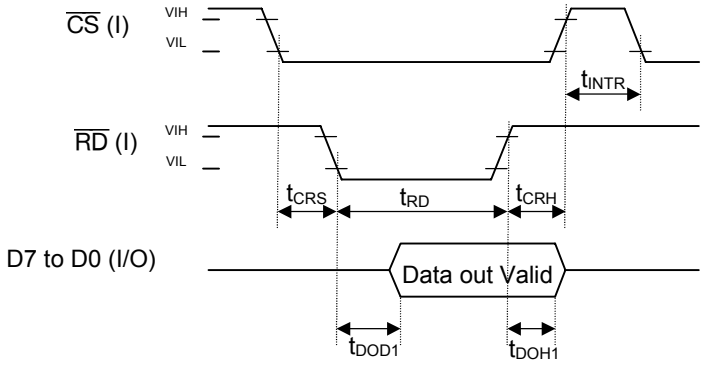
TIMING DIAGRAMS

Parallel CPU Interface Timing

- Data Write

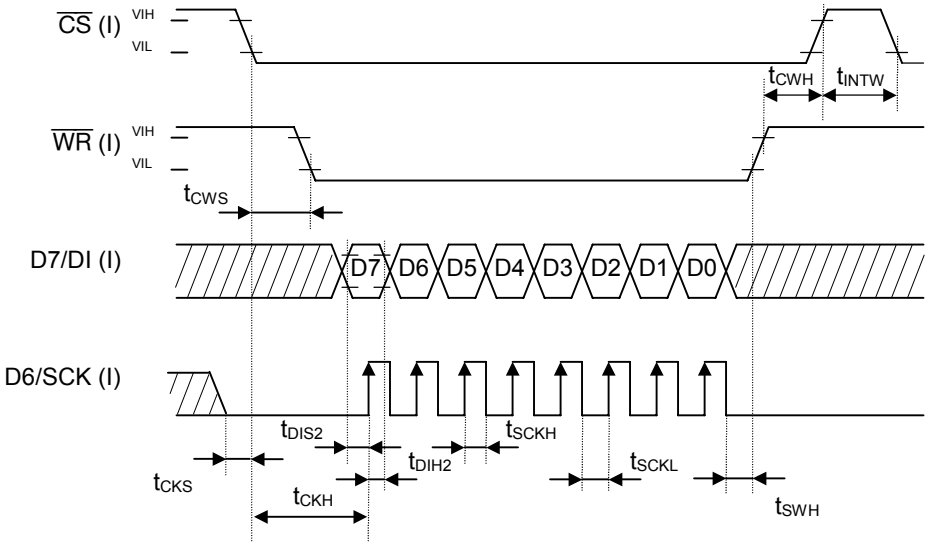


- Data Read

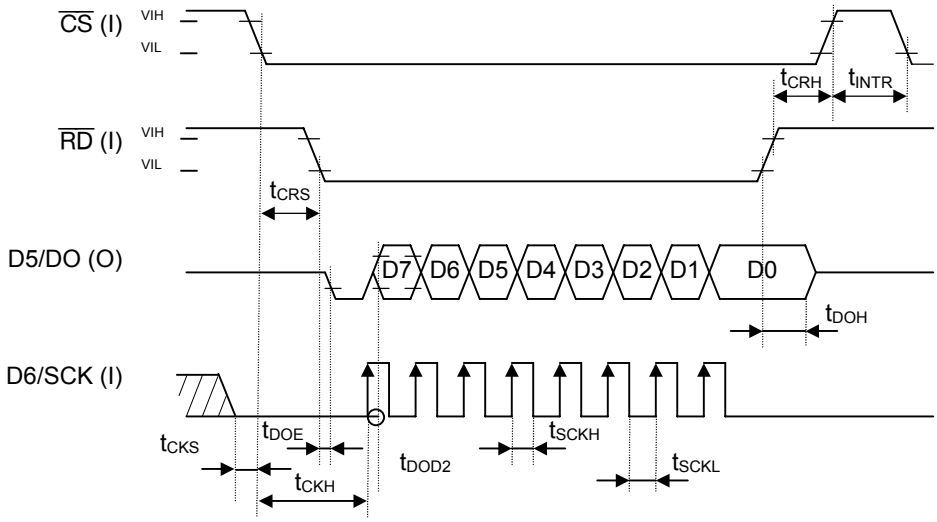


Serial CPU Interface Timing

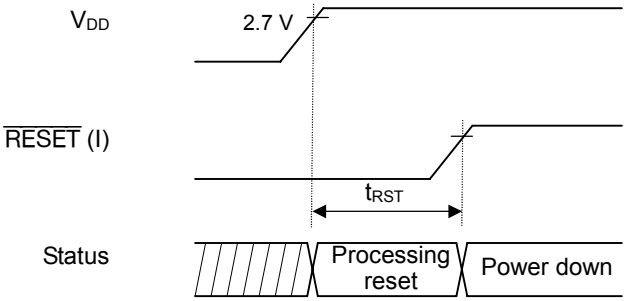
- Data Write



- Data Read

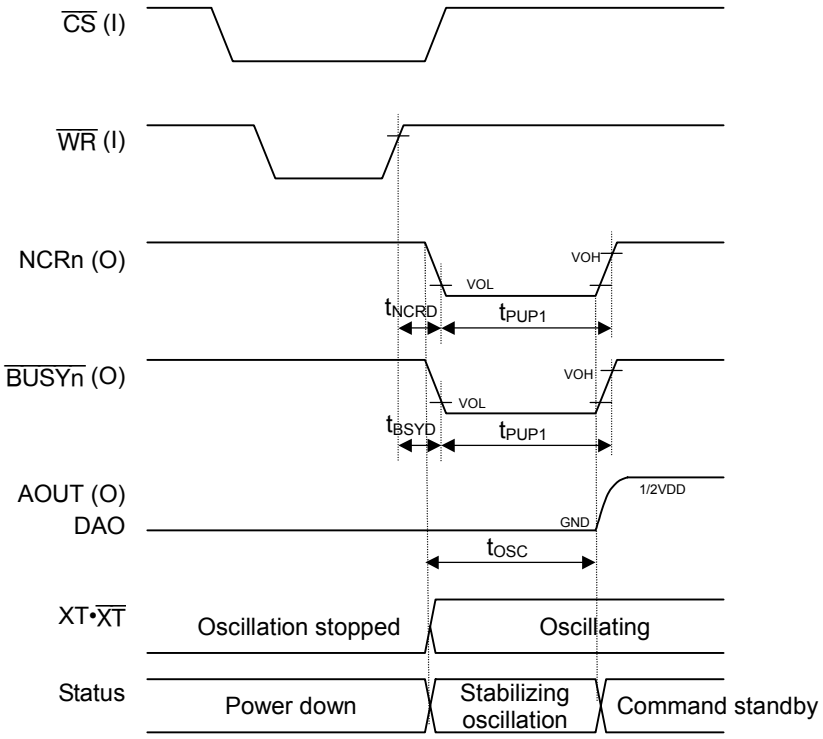


Power-On Timing



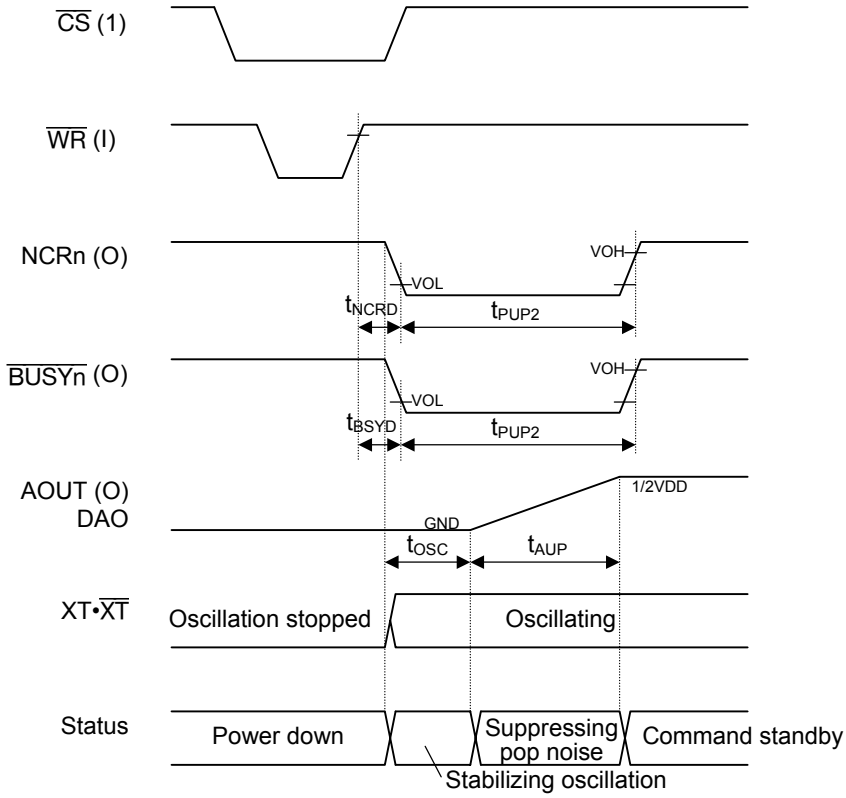
Power-Up Timing

- PUP1 command input



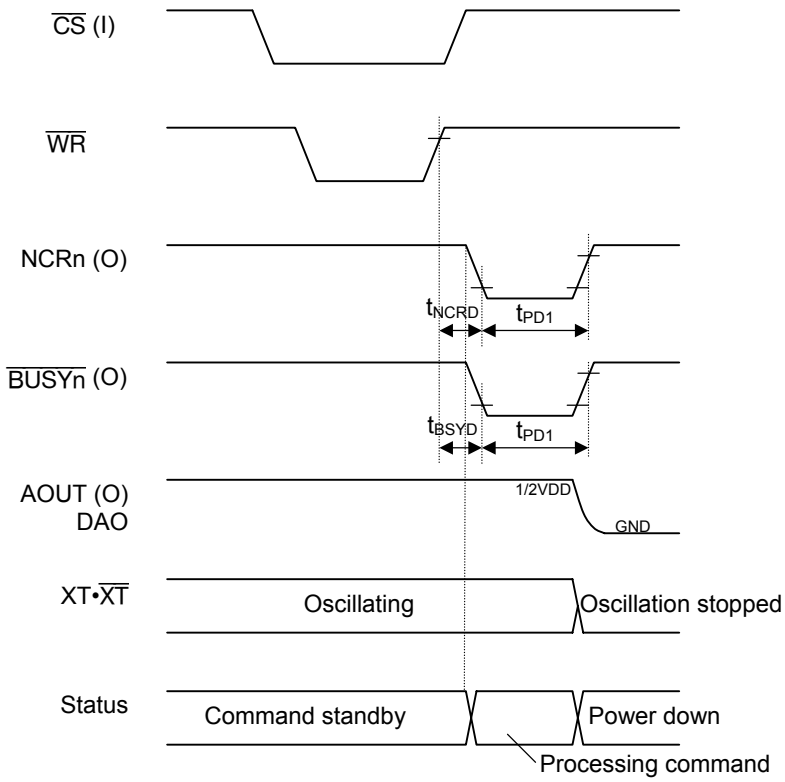
Note: The same timing at both parallel and serial interfaces.

• PUP2 command input



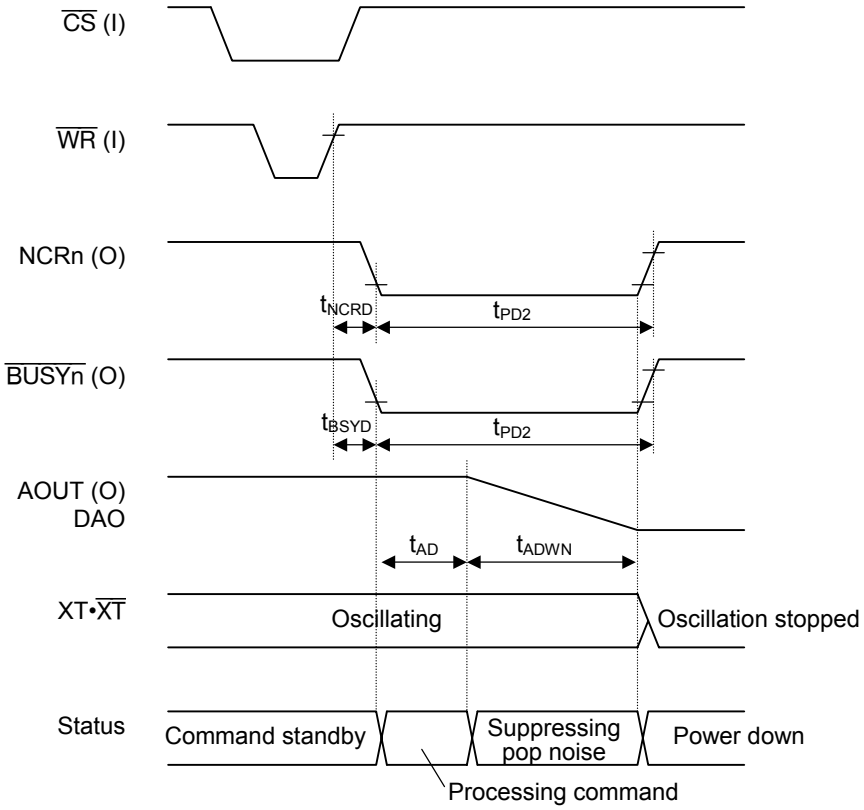
Power-Down Timing

- PDWN1 command input

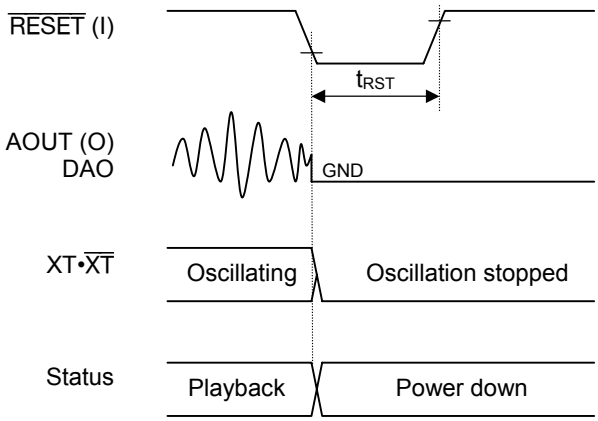


Note: The same timing at both parallel and serial interfaces.

• PDWN2 command input



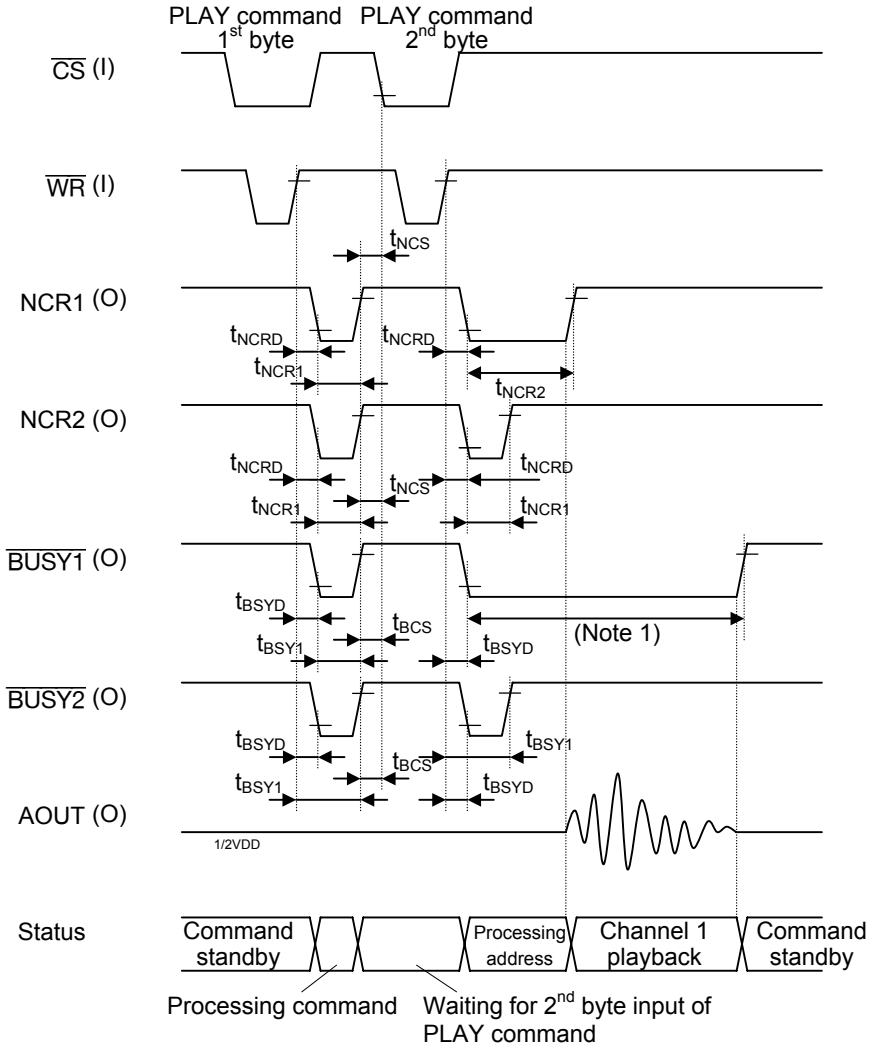
• RESET input



Note: The same timing even when RESET is input while waiting for command.

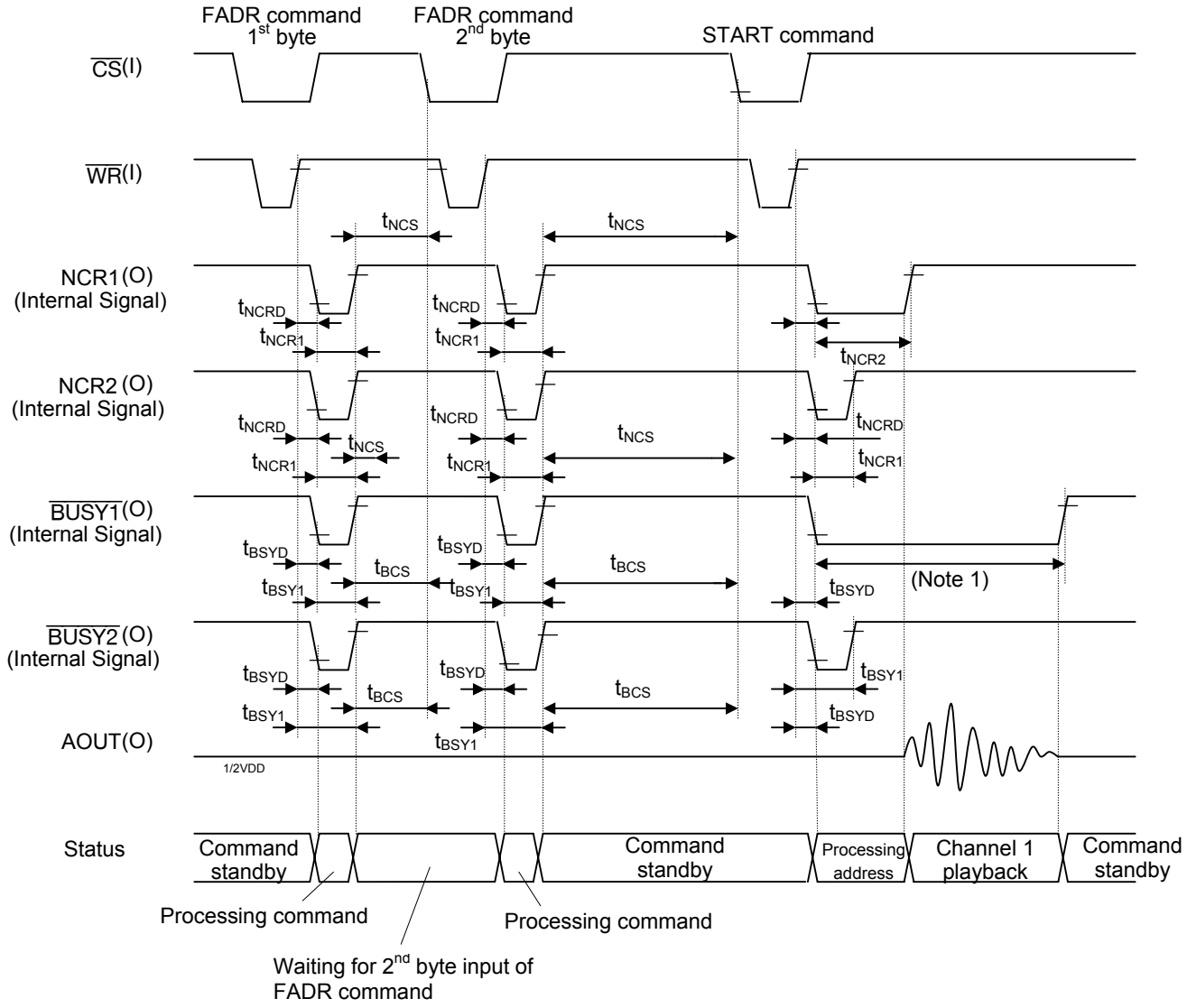
Single Channel Playback Timing

(Designated 1 channel and input the PLAY command when every channel does not playback.)

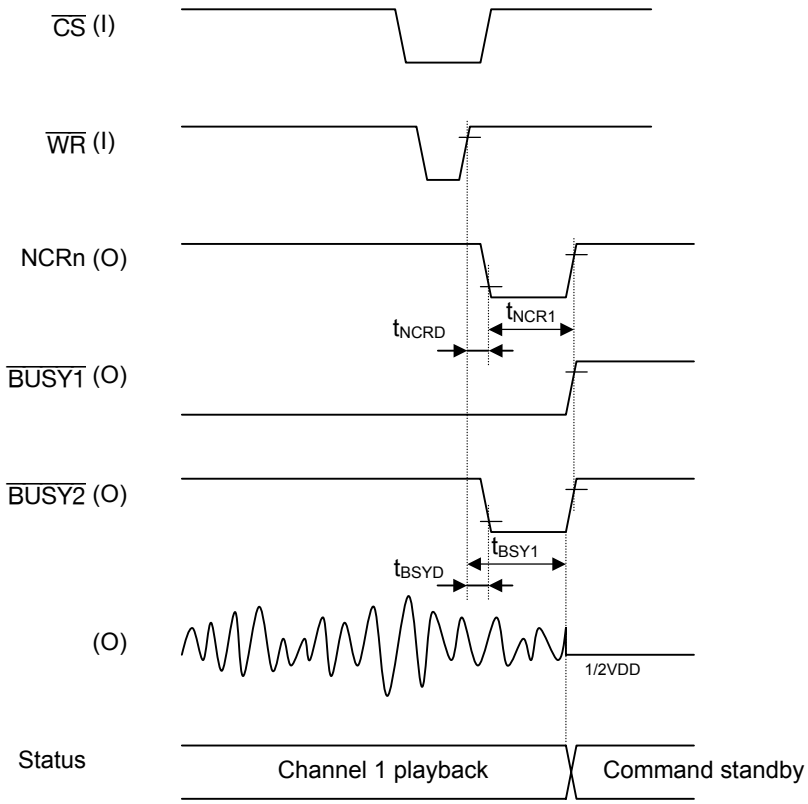


Note 1: Length of "L" interval of $\overline{\text{BUSY1}}$ is = t_{NCR2} + playback time length.
Note 2: The same timing at both parallel and serial interfaces.

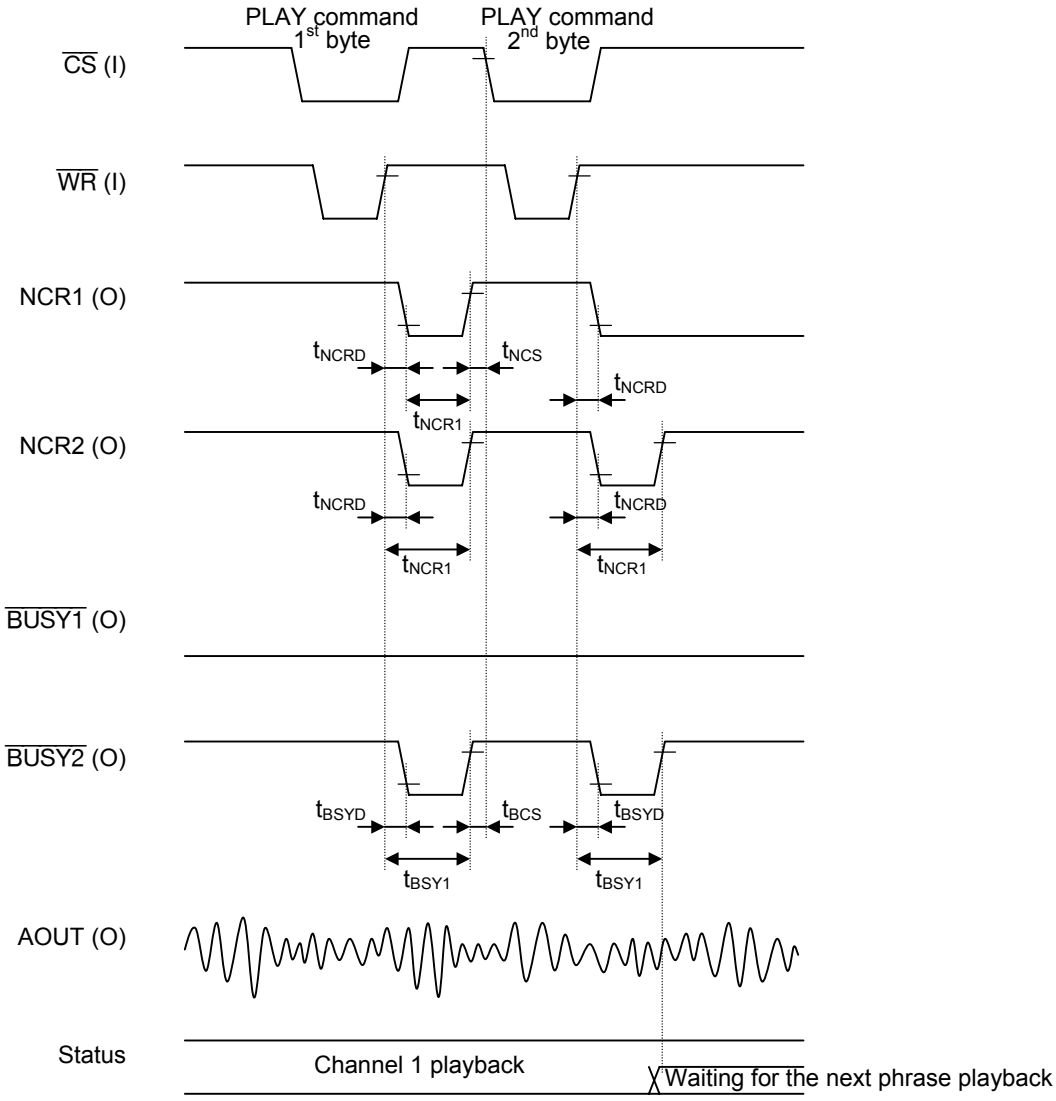
Single Channel Playback Timing by FADR, START command
(Channel 1)



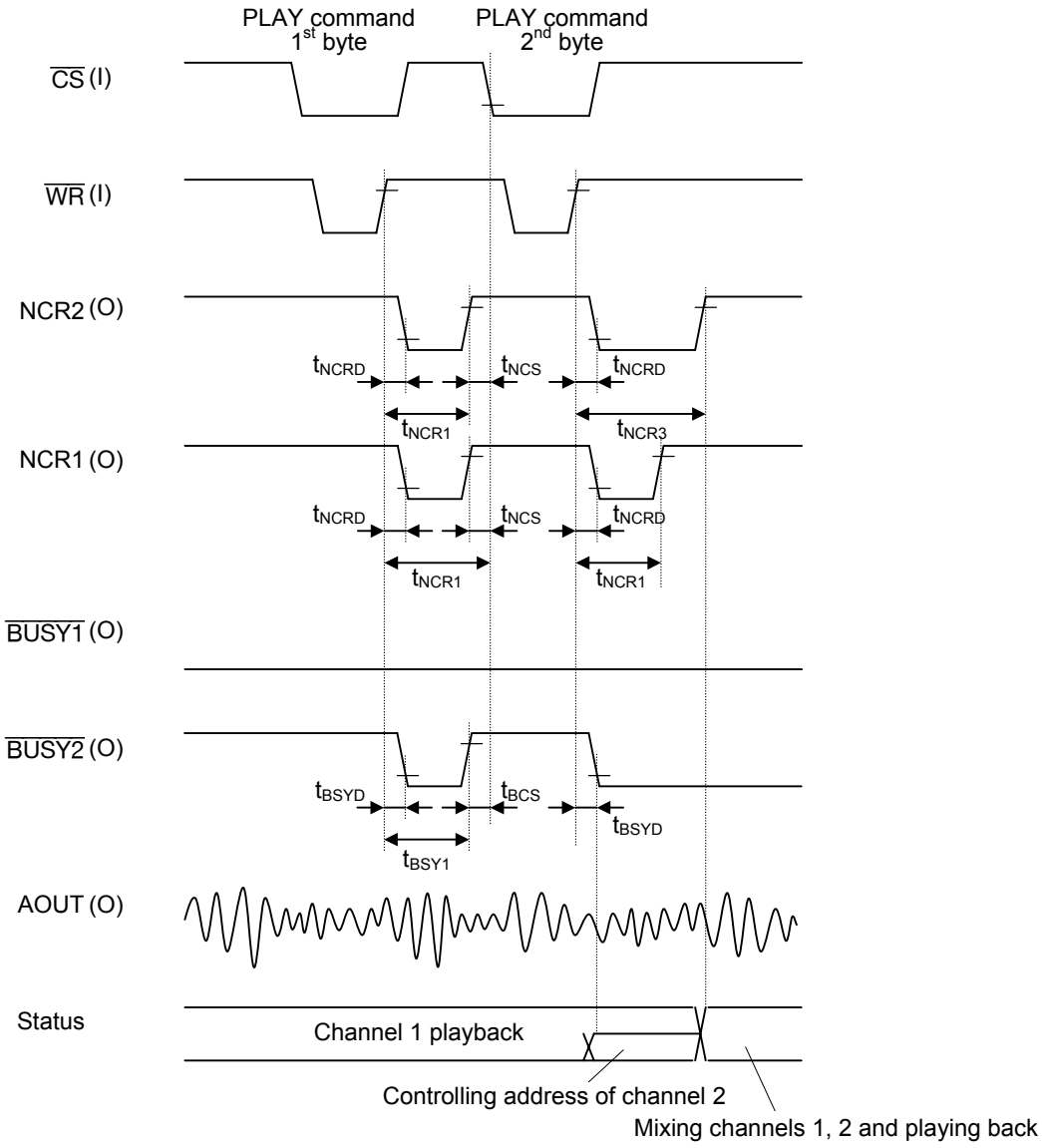
Playback Stop Timing (STOP command is input during channel 1 playback only.)



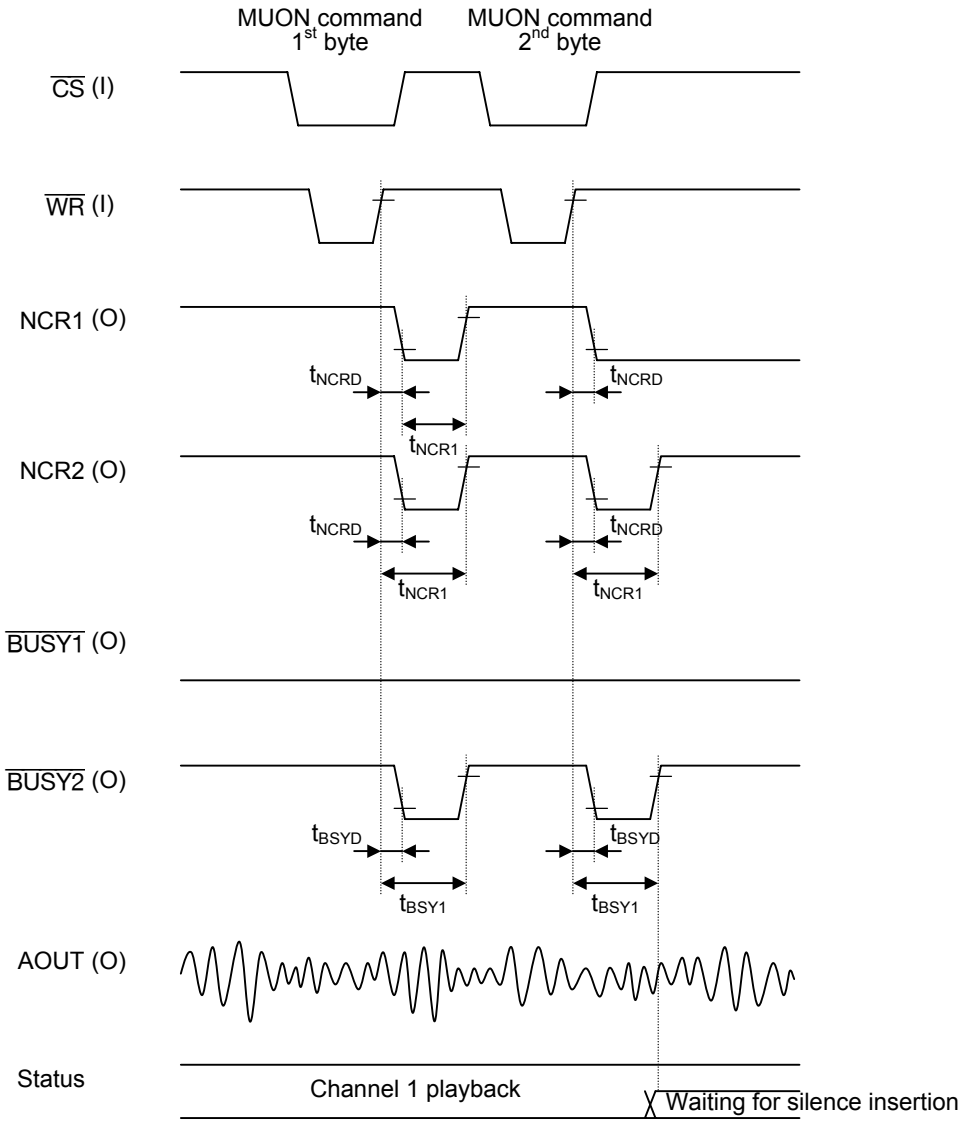
Single Channel Continuous Playback Timing (During channel 1 playback, designated channel 1 and input the PLAY command.)



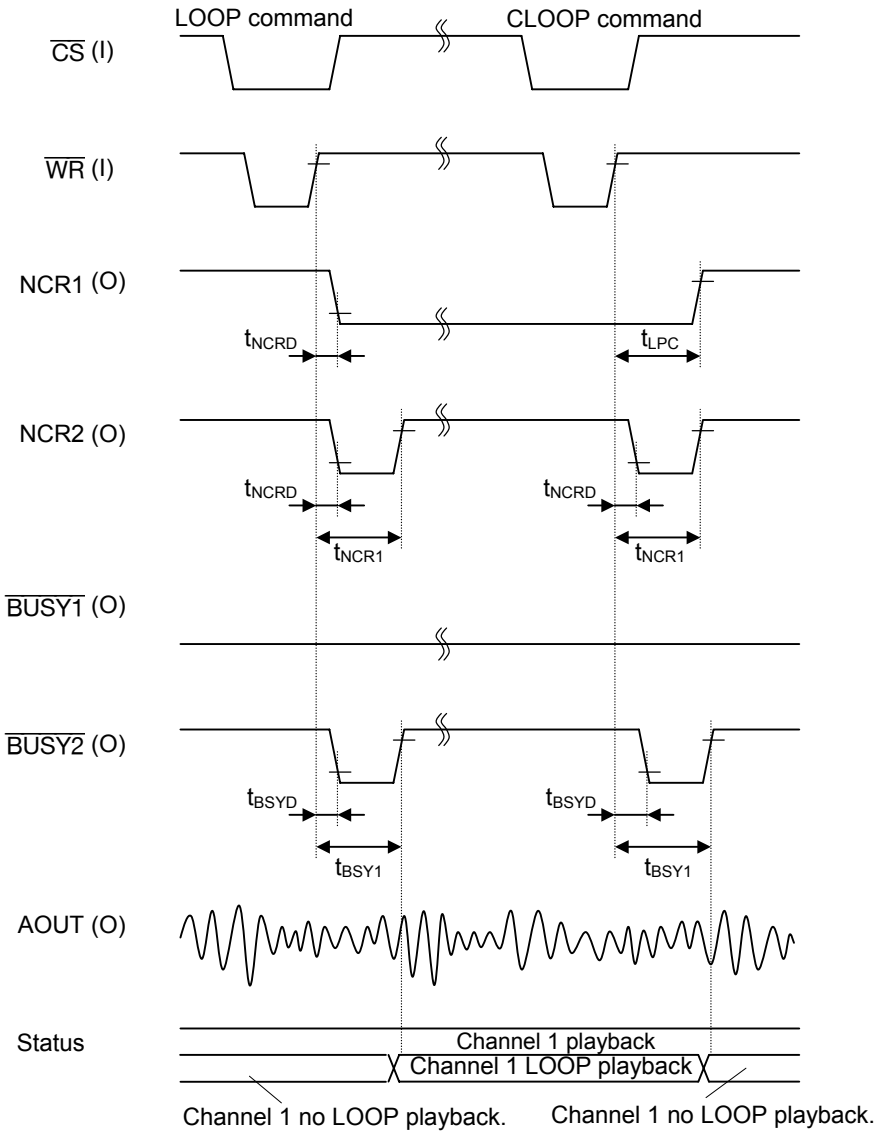
Mixing Playback Timing (During channel 1 playback, designated channel 2 and input the PLAY command.)



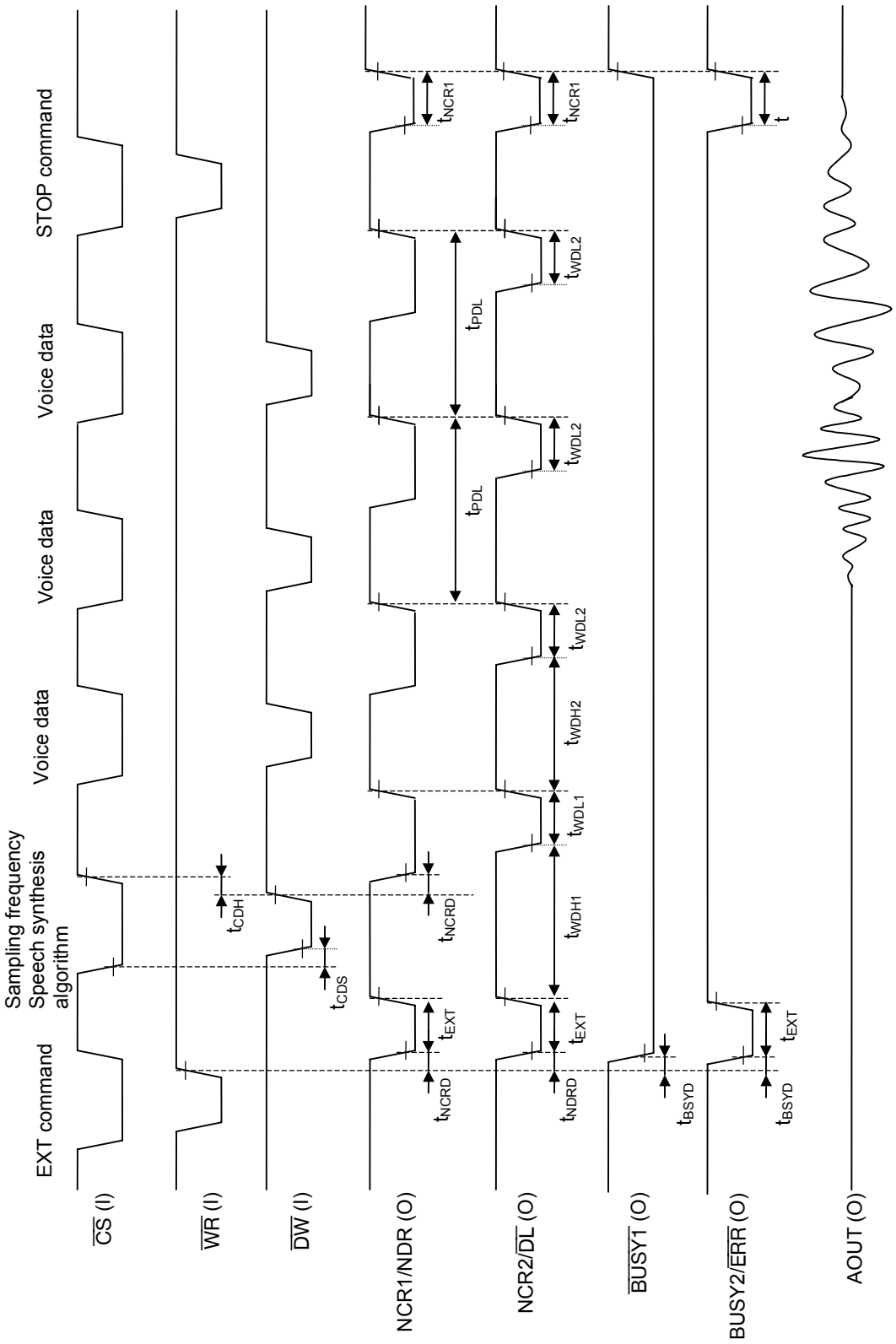
Silence Insertion Timing (MUON command is input during channel 1 playback)



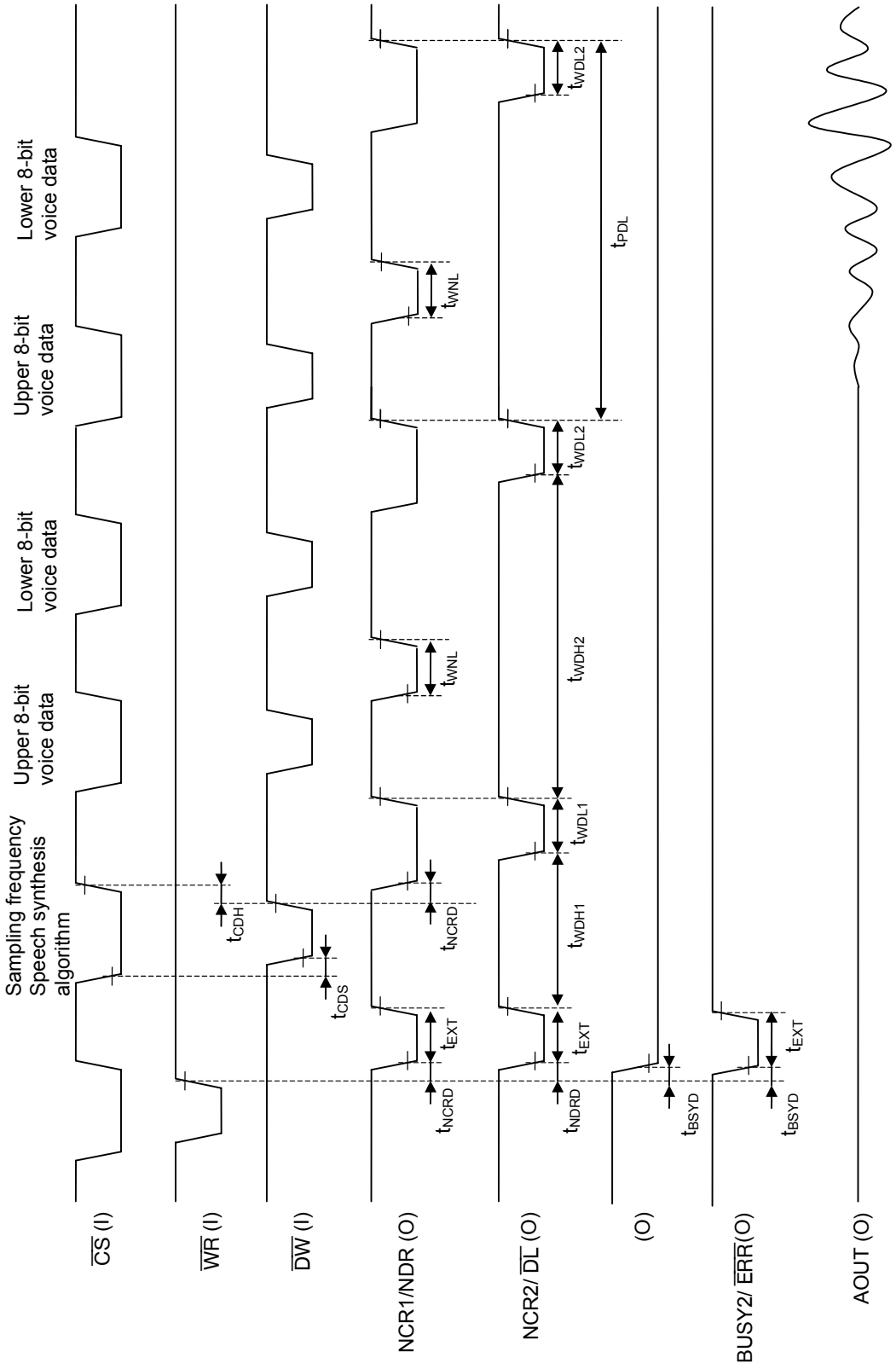
LOOP Playback Set/Release Timing (LOOP playback setting/releasing of channel 1 playback)



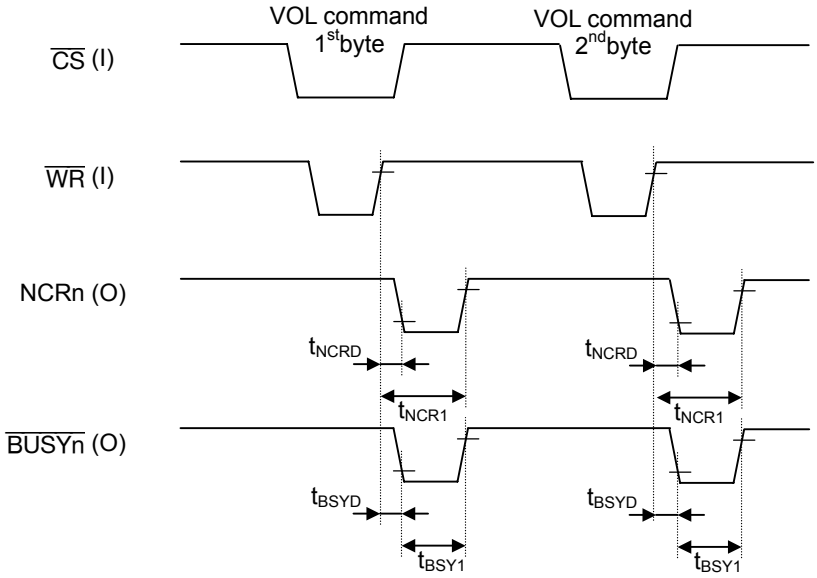
EXT Command Input Timing (16-bit PCM playback is excluded.)



EXT Command Input Timing (16-bit PCM playback)

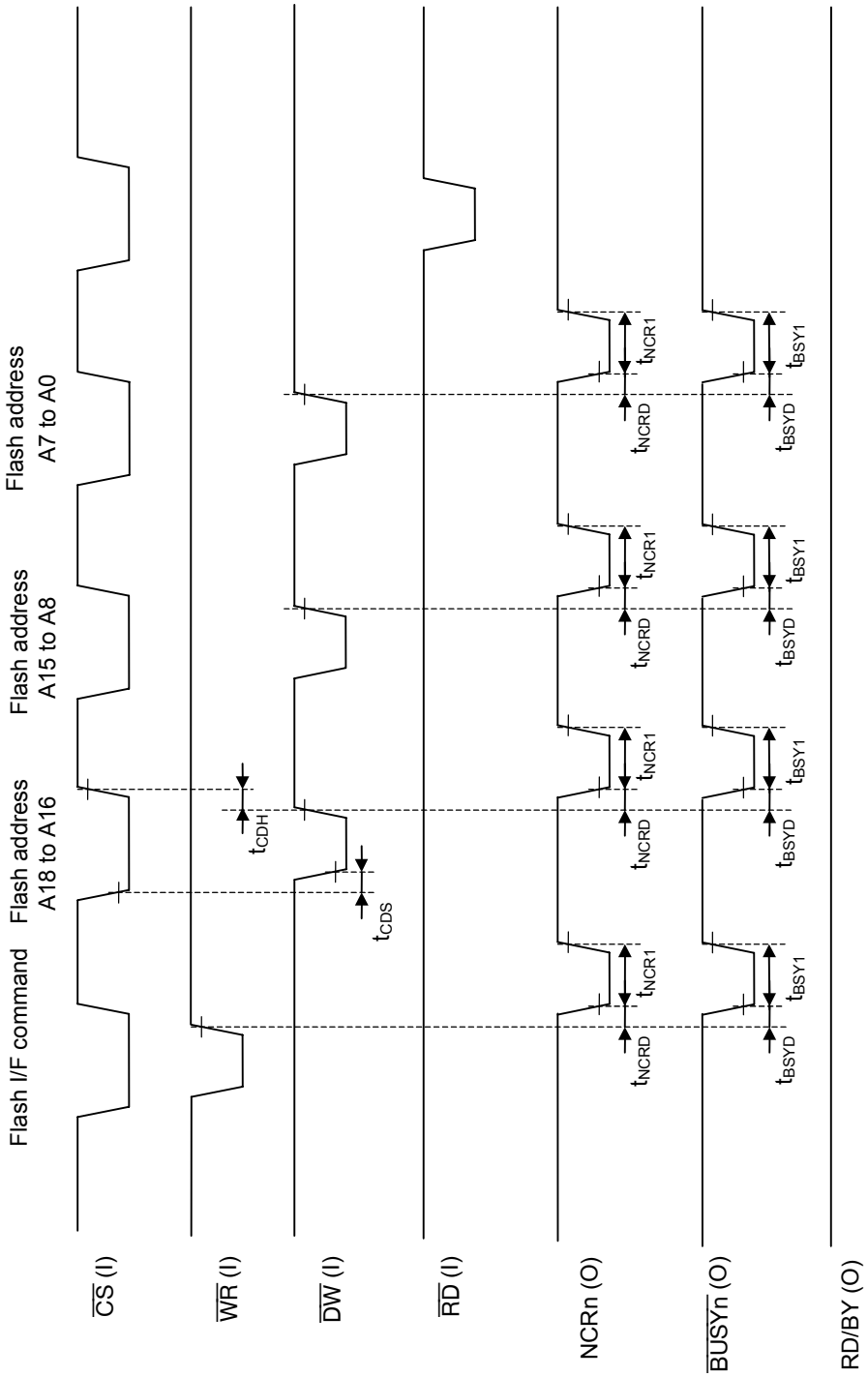


VOL Command Input Timing

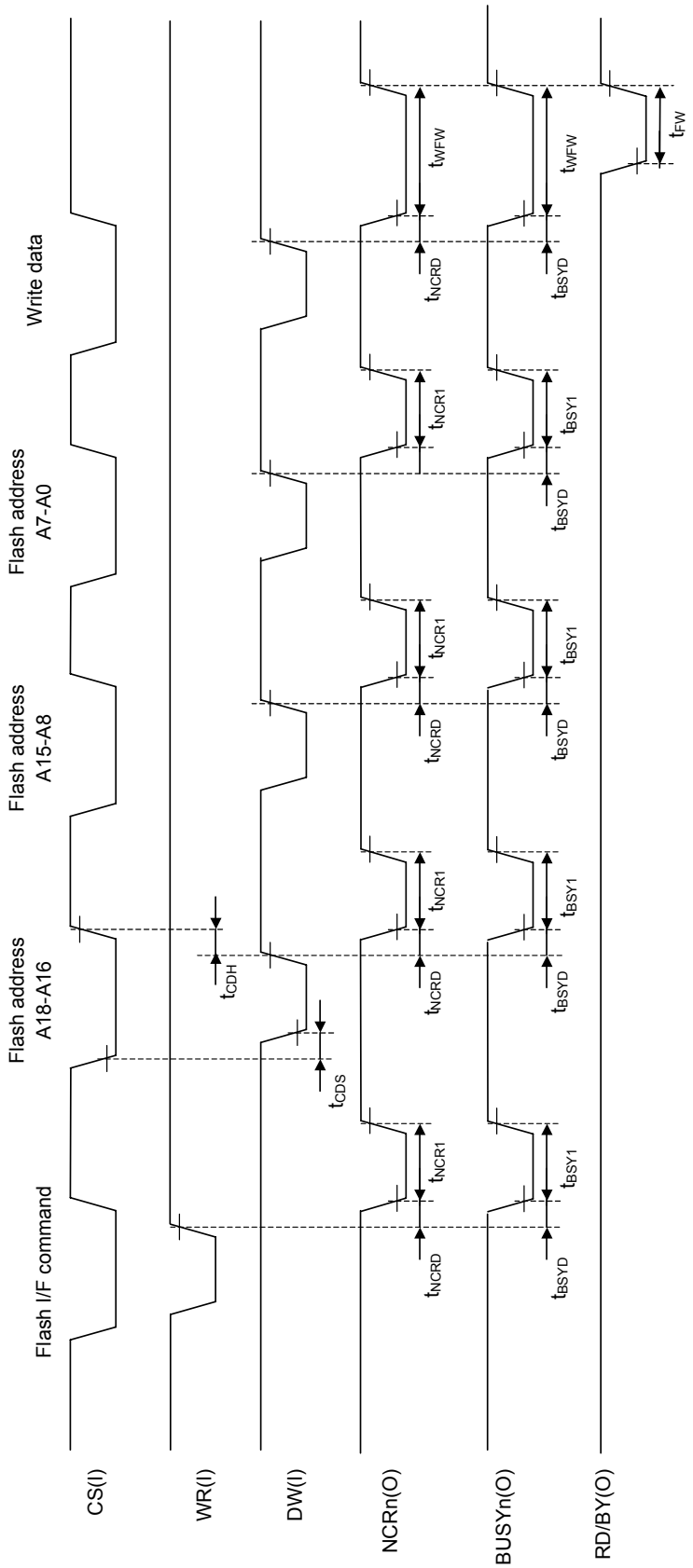


Flash I/F Command Input Timing

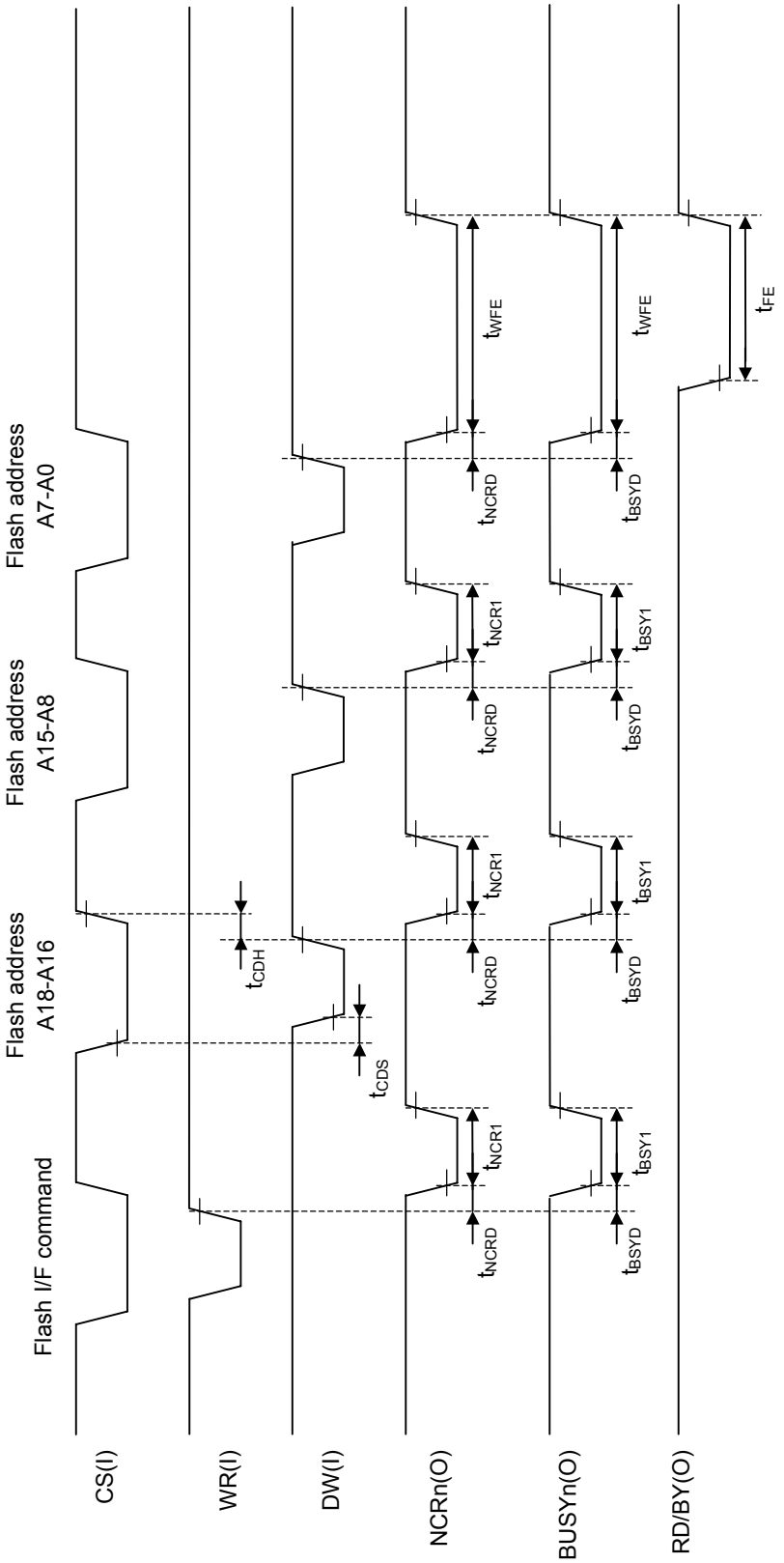
- Data Read Timing



- Data Write Timing



- Data Erase Timing



FUNCTIONAL DESCRIPTION

Micro-computer Interface

The micro-computer interface in the ML2250 family has 2 types of interface circuits built in: Parallel interface and serial interface. The interface setting can be changed with the SERIAL pin.

SERIAL pin = "H" level: Serial interface

SERIAL pin = "L" level: Parallel interface

Table below shows the SERIAL pin status in the serial and parallel interfaces.

SERIAL = "L"		SERIAL = "H"	
Parallel interface		Serial interface	
D7 (I/O)	Data input/output pins	D (I)	Serial data input pin
D6 (I/O)		SCK (I)	Serial clock input pin
D5 (I/O)		DO (O)	Serial data output pin
D4 (I/O)		D4 (I)	Not used. (Input "L" level.)
D3 (I/O)		D3 (I)	Not used. (Input "L" level.)
D2 (I/O)		D2 (I)	Not used. (Input "L" level.)
D1 (I/O)		D1 (I)	Not used. (Input "L" level.)
D0 (I/O)		D0 (I)	Not used. (Input "L" level.)

1. Parallel Interface

   When selecting the parallel interface, the I/O pins CS, WR, DW, D7 to D0, and RD are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data input.

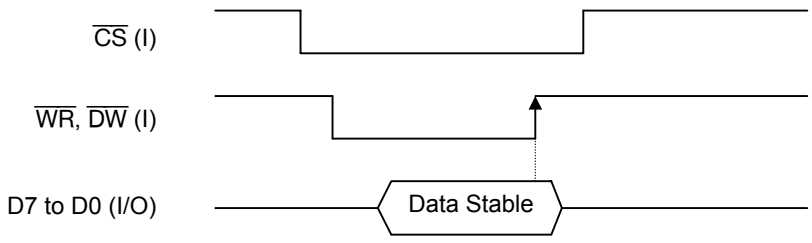
   The micro-computer interface becomes effective when the CS pin is set to "L" level.

   When a command or data is input, the input data to D7 through D0 pins is captured inside the device on the rising edge of the WR pin.

   The DW pin is used to input data after having input the EXT or Flash I/F command. The method to input data to the DW pin is the same as the method to input command from the WR pin.

   To read the channels status, pins CS and RD are made "L" level. By doing so, the status signals (NCR1, NCR2, BUSY1, BUSY2) of each channel are output to D3 through D0 pins. D7 to D4 pins usually output "L" level.

Command and Data Input Timing



Status Read Timing

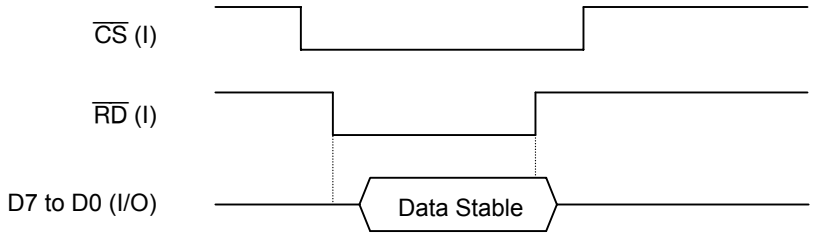


Table below shows the contents of each data output when reading the status of the channels.

Pin	Output status signal
D7	"L" level
D6	"L" level
D5	"L" level
D4	"L" level
D3	Channel 2 busy output ($\overline{\text{BUSY2}}$)
D2	Channel 1 busy output ($\overline{\text{BUSY1}}$)
D1	Channel 2 NCR output (NCR2)
D0	Channel 1 NCR output (NCR1)

The BUSY signal outputs "L" level when either a command is being processed or the playback of a pertinent channel is going on. In other states, the BUSY signal outputs "H" level.
The NCR signal outputs "L" level when either a command is being processed or a pertinent channel is in standby for playback. In other states, the NCR signal outputs "H" level.
To read out a status after inputting Flash I/F command for ML22Q54/Q58, D7-D0 pins output "L" level during command processing. After the command processing is completed, D7-D0 pins output "H" level.

2. Serial Interface

When selecting the serial interface, the I/O pins CS, WR, DW, DI, SCK, RD, and DO are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data.

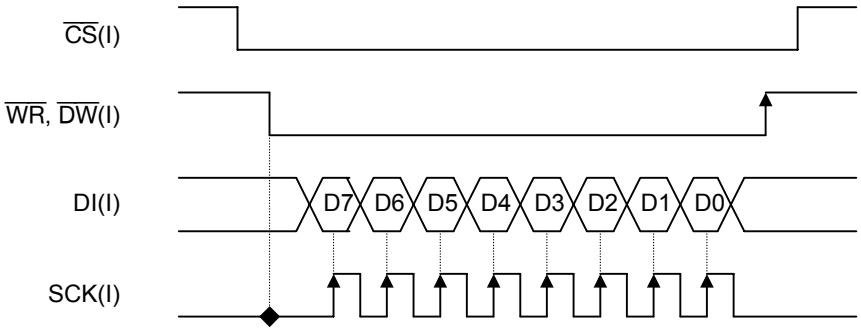
The micro-computer interface becomes effective when CS pin is set to "L" level.

To input the commands and data, "L" level is input to CS and WR pins followed by, from MSB, to DI pin in synchronization with the input clock signal at SCK pin. Data at DI pin is captured inside the device on the rising or falling edge of the clock at SCK pin. And the command is executed on the rising edge of the WR pin. The selection of rising/falling edge of SCK clock is determined by the input level of the SCK pin on the falling edge of the WR pin. If the SCK pin on the falling edge of the WR pin is at "L" level, the DI pin data is captured inside the device on the rising edge of SCK clock. Conversely, if the SCK pin on the falling edge of the WR pin is at "H" level, then the DI pin data is captured on the falling edge of SCK clock.

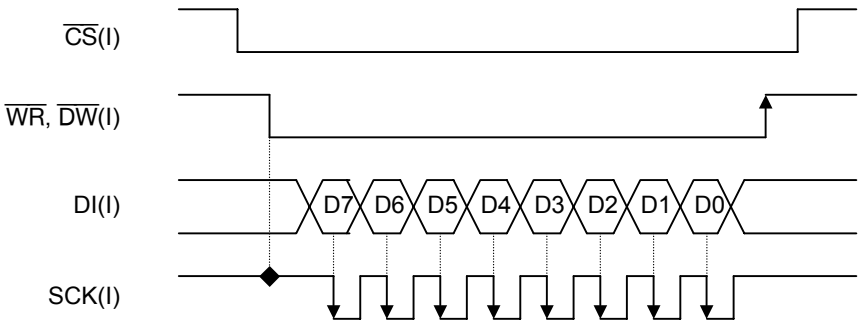
Use the DW pin to input various data after having input the EXT or Flash I/F command. The data input method is the same as to input data from the WR pin.

Command and Data Input Timings

- SCK Rising Edge Operation



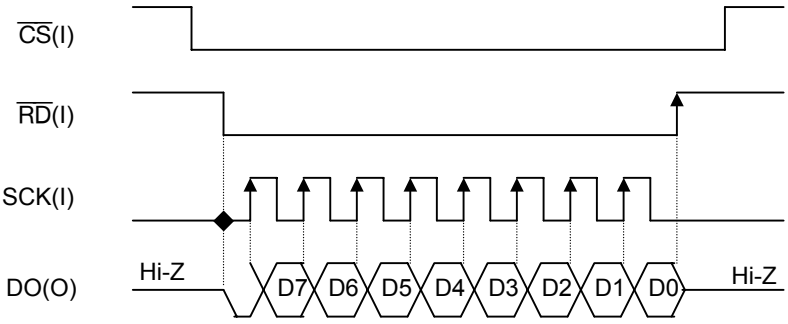
- SCK falling Edge Operation



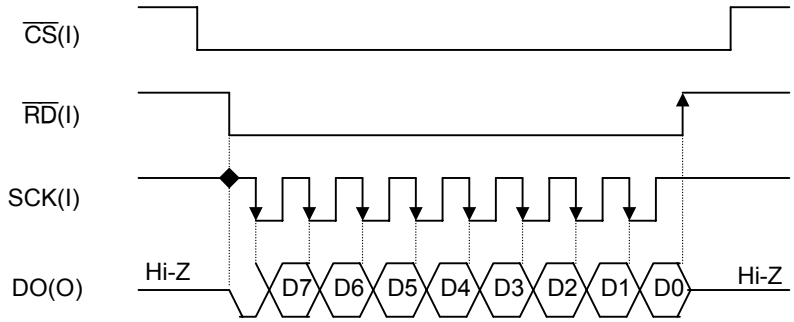
To read the channel status, input “L” level to CS and RD pins. DQ pin will output the channel status in synchronization with SCK clock.
The selection of rising/falling edge of SCK clock, similar to when inputting the commands and data, is determined by the level at SCK pin at the falling edge of RD pin.
The status signals in the parallel interface are output to D7 to D0 pins sequentially from D7.

Status Read Timing

- SCK Rising Edge Operation



- SCK Falling Edge Operation



Commands List

Each command is 1-byte (8 bits) input. PLAY, MUON, and FLASH I/F only are 2 bytes input.

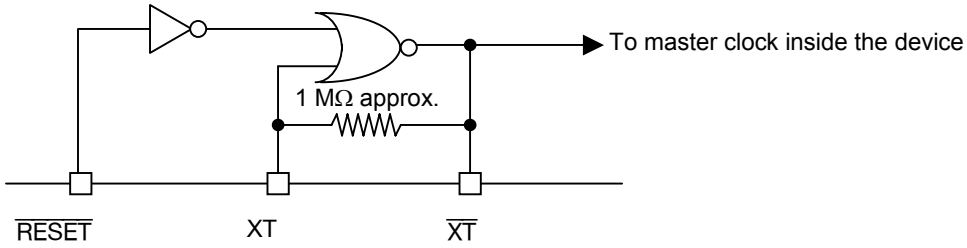
Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	0	0	0	0	Instantly shifts the power down device to the command standby state.
PUP2	0	0	0	1	0	0	0	0	Suppresses pop noise and shifts the power down device to the command standby state.
PDWN1	0	0	1	0	0	0	0	0	Instantly shifts the device from the command standby state to the power down state.
PDWN2	0	0	1	1	0	0	0	0	Suppresses pop noise and shifts the device from the command standby state to power down state.
PLAY	0	1	0	0	0	0	C1	C0	Inputs the phrase after the playback channel is specified, and then starts the playback.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	C1	C0	Playback start command with phrase specification. Inputs the phrase after the playback channel is specified, and then starts the playback. Playback start command without phrase specification. Inputs the phrase with the FADR command and starts the playback on multiple channels at the same time.
FADR	0	1	1	0	0	0	C1	C0	Phrase specification command. With this command, specifies the playback phrase for each channel.
	M7	M6	M5	M4	M3	M2	M1	M0	
STOP	0	1	1	1	0	0	C1	C0	Specifies the finish channel and ends the voice.
MUON	1	0	0	0	0	0	C1	C0	Inserts silence time after specifying the channel to insert silence, and then inserts silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	1	0	0	C1	C0	Repeats the playback mode setting command. Effective only for the channel being used for playback.
CLOOP	1	0	1	0	0	0	C1	C0	Repeat playback mode releasing command. Inputting the STOP command releases repeat playback mode automatically.
VOL	1	0	1	1	0	0	C1	C2	Specifies the channel whose sound volume is to be set, and then sets the volume of that channel.
	V7	V6	V5	V4	V3	V2	V1	V0	
EXT	1	1	0	0	0	0	0	0	Inputs voice data from the CPU I/F to play it back.
Flash I/F	1	1	0	1	BE	SE	WR	RD	Performs data read/write/erase of the built-in flash memory. This command cannot be used while the playback is going on. (Applicable to the ML22Q54/Q58.)

C1, C0: Channel specification (C0 = “1”: Channel 1; CH = “1”: Channel 2; C0, C1 = “1”: Channel 1, Channel 2)
F7 to F0: Phrase address
M7 to M0: Silence time length
X0: Releases the repeated playback
V4 to V0: Sound volume
RD, WR, SE, BE: Mode (RD = “1”: Read data; WR = “1”: Write data; SE = “1”: Erase sector; BE = “1”: Erase block)

Power Down Function

In power down state, the power down function in the device stops the internal operation and oscillation, sets AOUT to GND, and minimizes the static Idd.
When an external clock is in use, input "L" level to the XT pin, so that current does not flow into the oscillation circuit.

Figure below shows the equivalent circuit of XT and XT pins.



Initial state at the reset input
At the reset input, status of each output pins is described in the table below.

Output pin	Status	Output pin	Status
NCR1	"H" level	XT	"L" level
NCR2	"H" level	AOUT	"L" level
BUSY1	"H" level	DAO	"L" level
BUSY2	"H" level	VBG	"L" level
		REGOUT	Hi-z level

Channel Status

Channel status is of 2 types: NCRn and BUSYn.

Channel	Channel status	
CH1	NCR1	$\overline{\text{BUSY1}}$
CH2	NCR2	$\overline{\text{BUSY2}}$

NCRn = "H" indicates that it is possible to input the PLAY, START and MUON commands for the phrase to be played back next for channel n.

BUSYn = "H" indicates a state in which channel n has not performed voice processing. BUSYn = "L" indicates a state in which channel n is performing voice processing.
Meanwhile, after a command is input, the NCR and BUSY signals of all channels are at "L" level during the processing of the command.

Voice Synthesis Algorithm

The ML2250 family contains 5 algorithm types to match the characteristic of playback voice: 2-bit ADPCM 2 algorithm, 4-bit ADPCM 2 algorithm, 8-bit PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit PCM algorithm.
Key feature of each algorithm is described in the table below.

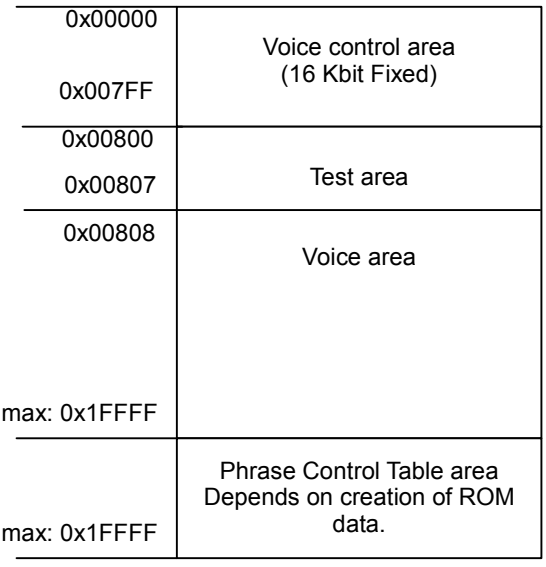
Voice synthesis algorithm	Applied waveform	Feature
Oki 2-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of low bit rate with improved 2-bit ADPCM.
Oki 4-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
Oki 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	High-frequency components inclusive sound effect etc.	Normal 8-bit PCM algorithm
16-bit PCM	High-frequency components inclusive sound effect etc.	Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into 4 data areas: voice (i.e., phrase) control area, test area, voice area, and phrase control table area.
The voice control area manages the ROM's voice data. It controls the start/end addresses of voice data, usage/not usage of the phrase control table function and so on. The voice control area stores voice control data for 256 phrases.
The test area stores the data for testing.
The voice area stores the actual waveform data.
The phrase control table area stores data for effective use of voice data. As for the details, please refer to the Phrase Control Table Function.
There is no phrase control table area if the phrase control table is not used.

The ROM data is created using a development tool.

ROM Addresses (ML2252)



Built-in ROM Usage Prohibited Area
(Applies to ML2251/52/53/54/56-XXX, ML22Q54/Q58)

The 8 bytes between the voice control area and the voice area in the ROM is the prohibited area for use.
The voice data are stored automatically behind 00808(HEX) address by using the development tool (AR207) when creating the ROM data.
Table below lists the addresses prohibited for use in every ROM model.

Model	Voice data area	Usage prohibited area
ML2251	00808 to FFFF	00800 to 00807
ML2252	00808 to 1FFFF	00800 to 00807
ML2253	00808 to 5FFFF	00800 to 00807
ML2254, 22Q54	00808 to 7FFFF	00800 to 00807
ML2256	00808 to BFFFF	00800 to 00807
ML22Q58	00808 to FFFFF	00800 to 00807

Note: The addresses are indicated in hexadecimal notation.

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 16)\ (\text{Kbit})}{\text{Sampling frequency (kHz)} \times \text{Bit length}}$$

(Bit length is ADPCM, ADPCM 2 = 4 bits; PCM = 8 bits.)

Example: Let the sampling frequency is 16 kHz and 4-bit ADPCM algorithm. If one 8 Mbits ROM is used, then the playback time is obtained as follows:

$$\text{Playback time} = \frac{1.024 \times (8192 - 16)\ (\text{Kbit})}{16\ (\text{kHz}) \times 4\ (\text{bit})} \cong 131\ (\text{sec})$$

The above equation gives the playback time when the phrase control table function is not used.

Mixing Function

The ML2250 family can perform simultaneous mixing of 2 channels. It is possible to specify PLAY and STOP for each channel separately.

- Precautions for Waveform Clamp at the Time of Channels Mixing
  When mixing of channels is done, the clamp occurrence possibility increases from the mixing calculation point of view. If it is known beforehand that the clamp will occur, then adjust the sound volume by VOL command.

- Mixing of Different Sampling Frequency
  It is not possible to perform analog mixing by a different sampling frequency.
  When performing analog mixing, the sampling frequency group of the first playback channel is selected. Therefore, please note that if analog mixing is performed by a sampling frequency group other than the selected sampling frequency group, then the playback will not be of constant speed: some times faster and at other times slower.
  The available sampling groups for analog mixing by a different sampling frequency are listed below.
  4.0 kHz, 8.0 kHz, 16.0 kHz, 32.0 kHz ··· (Group 1)
  5.3 kHz, 10.6 kHz, 21.3 kHz, 42.7 kHz ··· (Group 2)
  6.0kHz, 12.0kHz, 24.0kHz, 48.0kHz ··· (Group 3)
  6.4 kHz, 12.8 kHz, 25.6 kHz ··· (Group 4)

Figures below show a case when a sampling frequency group played back a different sampling frequency group.

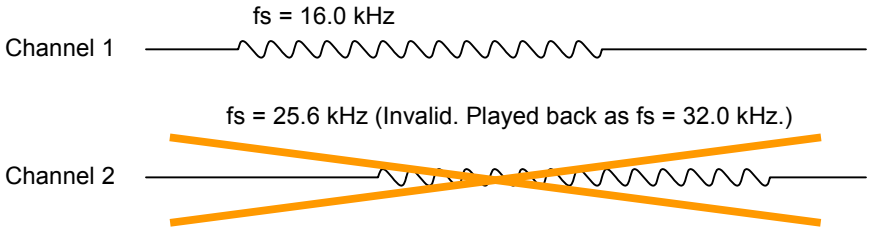


Figure 1 In Case a Different Sampling Frequency Played Back during Playback of the Other Channel Playback

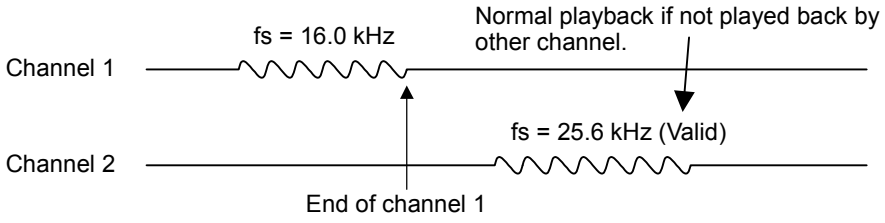


Figure 2 In Case a Different Sampling Frequency Played Back after the End of the Other Channel

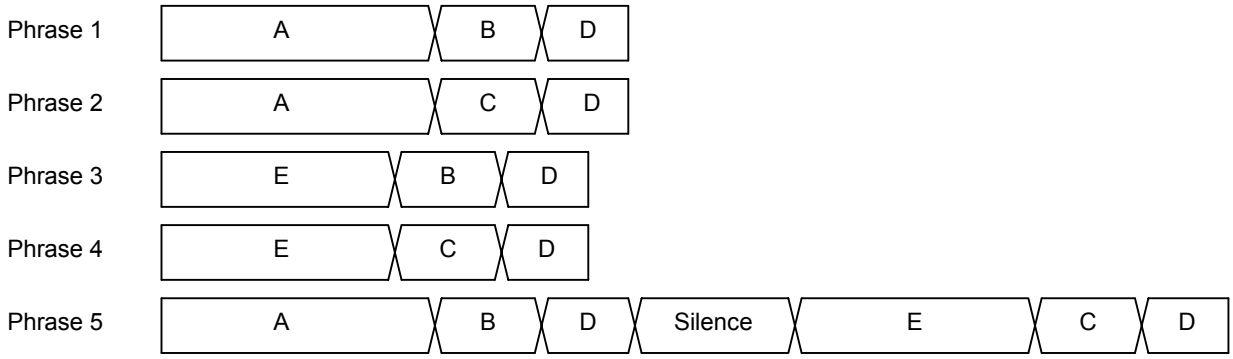
Phrase Control Table Function

The phrase control table function makes it possible to play back multiple phrases in succession. The following functions are set using the phrase control table function:

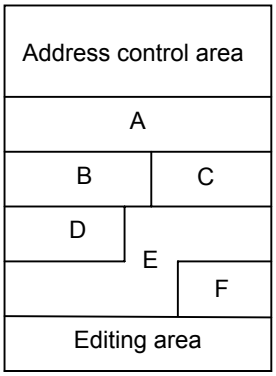
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 4 to 1024 ms

Using the phrase control table function enables to effectively use the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the phrase control table function.

Example 1: Phrases Using the Phrase Control Table Function



Example 2: Example of ROM Data in case Example 1 Converted to ROM



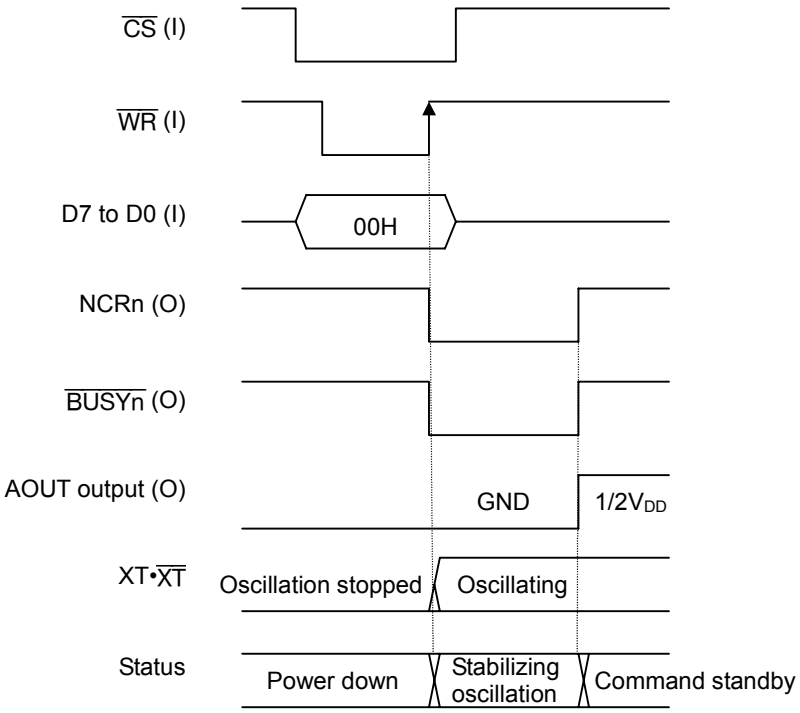
Command Function Descriptions

1. PUP1 Command

• command	0	0	0	0	0	0	0	0

PUP1 command is used to shift the ML2250 family from power down state to the command standby state.
In the power down state, since the ML2250 family can receive either PUP1 or PUP2 command only, the device will ignore any other input command.
The ML2250 family enters into the power down state in any of the following 3 conditions:

1) When the power is inserted.
2) At RESET input
3) When NCRn and BUSYn go "H" level after inputting the power down command.



The oscillation starts on the rising edge of WR and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output abruptly changes from GND level to $1/2V_{DD}$ level. Therefore, this abrupt change in AOUT output will cause to generate the pop noise if the AOUT output is not processed outside. To suppress the pop noise, input the PUP2 command.
In the case of serial interface also, the oscillation starts on the rising edge of WR and, after an elapse of oscillation stabilization time, the AOUT output abruptly changes from GND level to $1/2V_{DD}$ level.

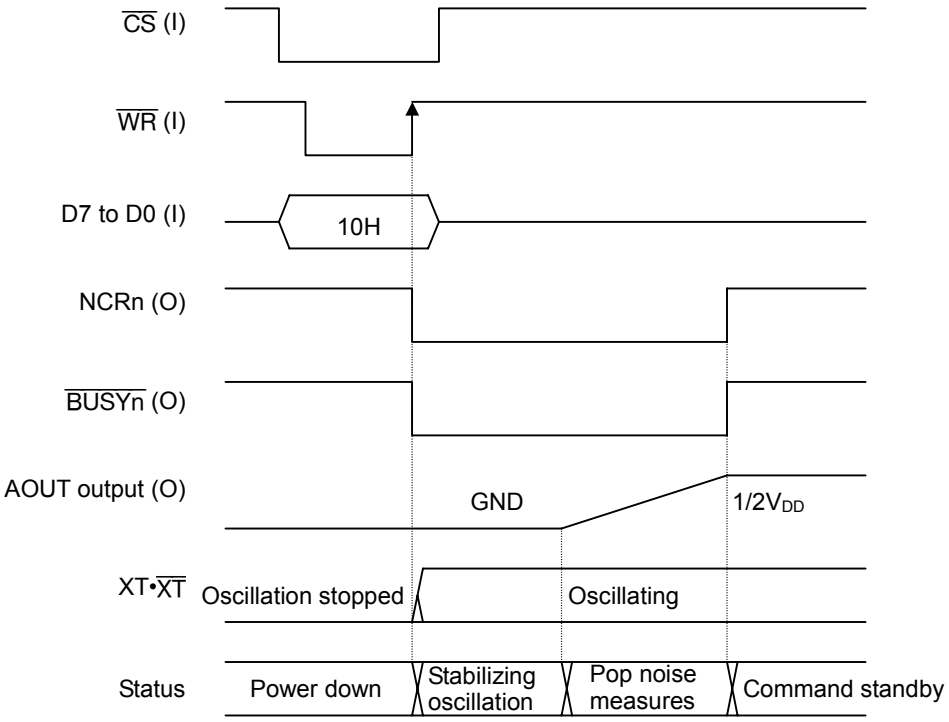
All commands that will be input during oscillation stabilization are ignored,
However, if RESET is input, ML2250 family soon enters the power down state.

2. PUP2 Command

• command	0	0	0	1	0	0	0	0

PUP2 command is used to take measures for the pop noise from the power down state and to shift the ML2250 family to the command standby state.
Since ML2250 family receives either PUP1 or PUP2 command only in the power down state, it will ignore any other command input.
The ML2250 family enters into the power down state in any of the following 3 conditions:

1) When the power is inserted.
2) At RESET input
3) When NCRn and BUSYn go "H" level after the power down command is input.



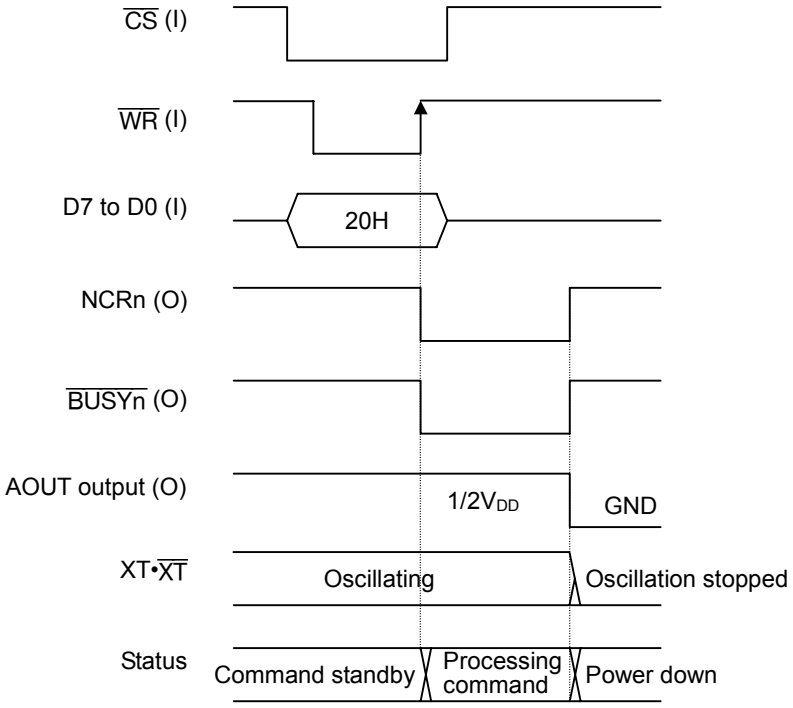
The oscillation starts with the rising edge of WR and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output gradually changes from GND level to $1/2V_{DD}$ level in about 64 ms.
In the case of serial interface also, the oscillation starts with the rising edge of WR and, after an elapse of oscillation stabilization time, the AOUT output gradually changes from GND level to $1/2V_{DD}$ level.

All commands that will be input during oscillation stabilization or while pop noise is being suppressed, are ignored. However, if RESET is input, the ML2250 family soon enters the power down state.

3. PDWN1 Command

• command	0	0	1	0	0	0	0	0

The PDWN1 command is used to shift the ML2250 family from command standby state (both NCRn and BUSYn are “H”) to the power down state.
To resume speech synthesis processing after the ML2250 family has shifted to the power down state, first input the PUP1 or PUP2 command and then input the PLAY command.



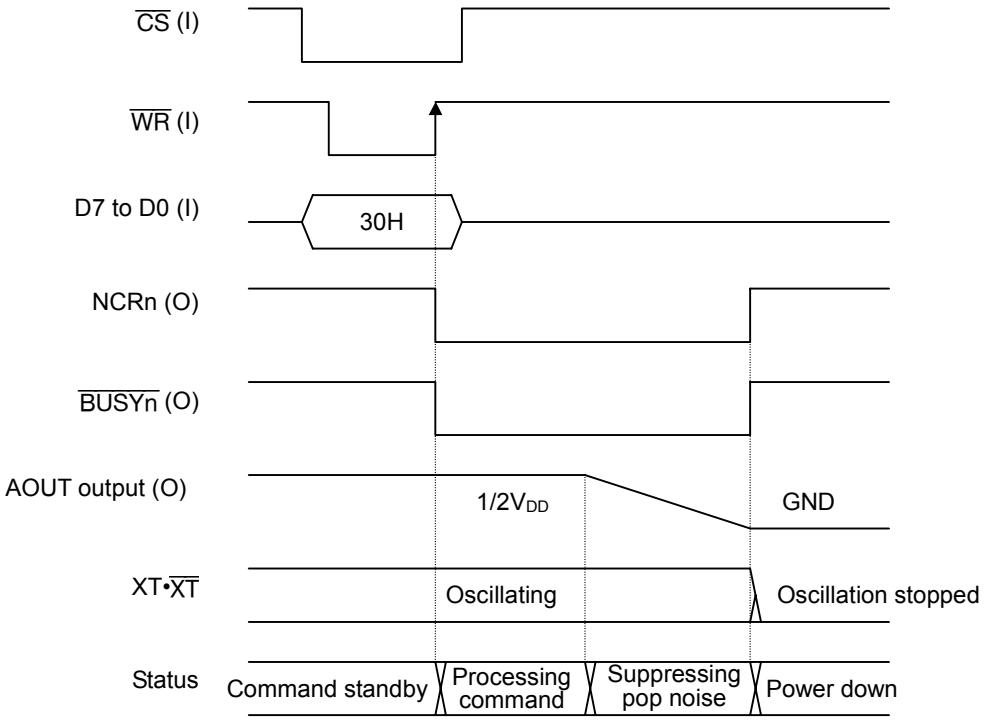
After the rising edge of WR and after an elapse of the PDWN1command processing time, the oscillation stops and the AOUT output abruptly changes from GND level to $1/2V_{DD}$ level. This abrupt change in the AOUT output will cause to generate pop noise if the AOUT output is not processed outside. To suppress pop noise, input the PDWN2 command.

The operation after the rising edge of WR is also the same as in the case of serial interface.

4. PDWN2 Command

• command	0	0	1	1	0	0	0	0

PDWN2 command is used to take measures for the pop-noise from the command standby status (both NCRn and BUSYn are "H") and to shift the ML2250 family to the power down state.
To resume speech synthesis processing after the ML2250 family has shifted to the power down state, first input the PUP1, or PUP2, command followed by the PLAY command.



After the rising edge of WR and the elapse of PDWN2 command processing time, the AOUT output changes gradually in 64 ms from $1/2V_{DD}$ level to GND level.
Also in the case of the serial input interface, the AOUT output changes gradually from $1/2V_{DD}$ level to GND level after the elapse of command processing time.

All commands that will be input while the pop noise is being suppressed, are ignored. However, if RESET is input, the ML2250 family soon enters the power down state.

5. PLAY Command

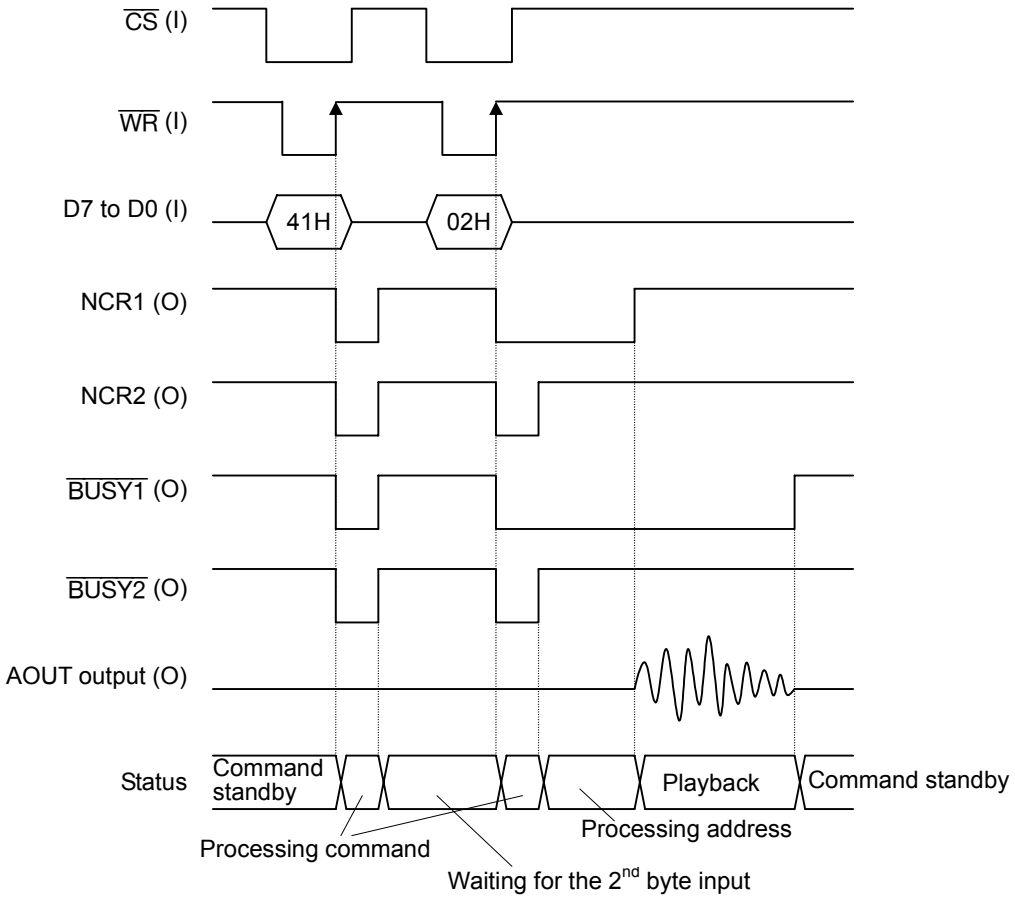
• command

0	0	0	0	0	1	C1	C0	1 byte
F7	F6	F5	F4	F3	F2	F1	F0	2 bytes

PLAY command is a 2-byte command. The command first specifies the playback channel, and next sets the playback phrase. PLAY command should be input during the NCR signal of the playback channel is on the "H" level.

C1	C0	Description
0	1	Starts playback of channel 1.
1	0	Starts playback of channel 2.

Since it is possible to specify the playback phrase (F7 to F0) at the time of creating the ROM that stores voice data, please set the phrase that was set when the ROM was created.
Figure below shows the timing of phrase (F7 to F0 = 02H) playback by channel 1.



When the 1st byte of the PLAY command is input, the device enters a state in which it waits for the 2nd byte to input after the elapse of the command processing time. When the 2nd byte of PLAY command is input then, after an elapse of the command processing time, the device starts reading from the address information ROM of phrase for playback by channel 1. Thereafter, channel 1 starts the playback operation, the playback is performed up to the specified ROM address, and then the playback ends automatically.
NCR1 signal of channel 1 remains "L" level during the address control, and returns to "H" level when the address control is finished and the playback starts. When this NCR signal goes "H" level, then it is possible to input the PLAY command of the next playback phrase.
BUSY1 signal of channel 1 remains "L" level during the address control and while playback is going on, and returns to "H" level when the playback is finished. Whether the playback is going on can be known by the BUSY signal.

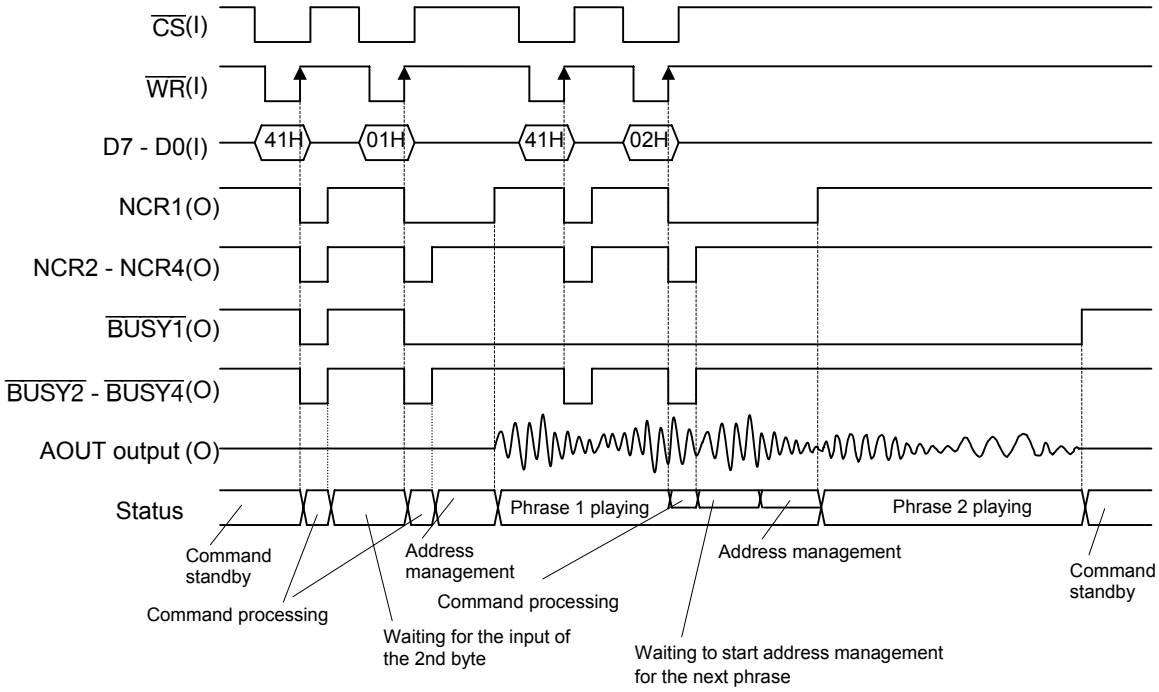
Address Management Time

The time required for managing the address of the playback phrase after the PLAY command is input depends on the lowest sampling frequency of the sampling frequency group that was used to playback the previous phrase. After power is turned on or after RESET is input, a sampling frequency of 4 kHz is used. The sampling frequency for the phrase played back the last time is effective irrespective of which playback channel is used. The table below shows the correspondence between the sampling frequency that was used to playback a phrase the last time and the time required for address management when playing back the next phrase.

Sampling frequency the last time the phrase was played back	Time required for address management when playing back the next phrase
4 kHz, 8 kHz, 16 kHz, 32 kHz	16 to 17 cycles of 4 kHz (4.00 ms to 4.25 ms)
5.3 kHz, 10.6 kHz, 21.3 kHz, 42.7 kHz	16 to 17 cycles of 5.3 kHz (3.00 ms to 3.19 ms)
6.4 kHz, 12.8 kHz, 25.6 kHz	16 to 17 cycles of 6.4 kHz (2.50 ms to 2.66 ms)
6.0kHz, 12.0kHz, 24.0kHz, 48 kHz	16 to 17 cycles of 6 kHz (2.66 ms to 2.84 ms)

PLAY Command Input Timing for Continuous Play

The diagram below shows the input timing for the PLAY command when a phrase is played on a channel in continuation of the phrase that preceded it.



The ML2240 synchronizes the address management for the second phrase with the sampling cycle of the phrase that is playing. As shown in the diagram above, when the PLAY command for the second phrase is input, the status is changed to "waiting to start address management for the next phrase." When the remaining voice data of the phrase that is playing reaches the amount of sampling cycles required for address management, the address management for the second phrase begins.
This process makes it possible for the second phrase to start playing back immediately after the first phrase finishes. Phrases can thus be played back continuously without inserting silence between phrases.
However, if the play command for the second phrase is input after there are too few sampling cycles of voice data remaining in the first phrase to allow the address management of the second, the address management of the second phrase will not be completed when the first phrase finishes playing back. Silence is inserted in the interval from the time the address management is completed to when the second phrase begins to play back.

The table below shows the play command input timing for the next phrase continuous play back without the insertion of silence between the phrases using the amount of remaining voice data (the number of samples) in the currently playing back phrase.

Playback method	PLAY input timing Amount of remaining voice data in playing back phrase
2 bit Oki ADPCM2	69th sample or before
4 bit Oki ADPCM2	35th sample or before
8 bit nonlinear / 8bit PCM	18th sample or before
16 bit PCM	18th sample or before

If the PLAY command for the second phrase is input before the number of samples indicated in the table is reached, continuous play is achieved without the need to insert silence between phrases.

Notice of Continuous Play

In the case of continuous play using deference sampling frequencies , it may hear as noise on the joint of phrases. The noise is generated by changing cut off frequency built-in the digital filter, and the degree of noise depends on sound sources.
To decrease the noise, inputting 15 sampling or more silent data from the last data of a voice phrase.

In the case of continuous play using the same sampling frequency, the noise is not generated because cut off frequency built-in the digital filter doesn't change.

6. START Command

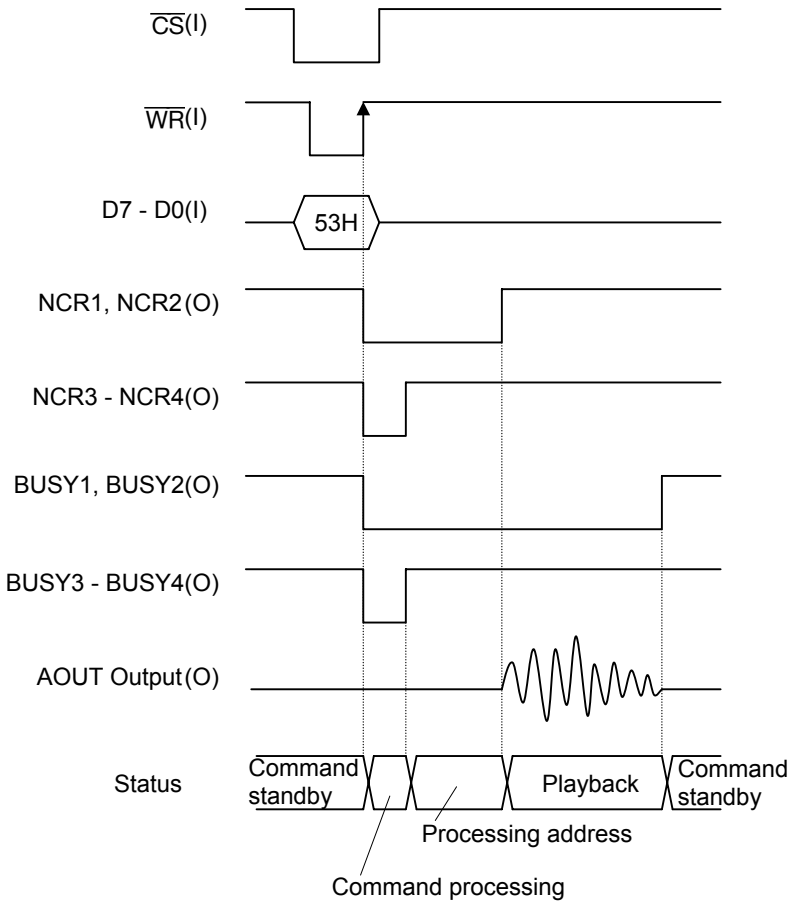
• command	0	1	0	1	0	0	C1	C0

Playback starts on the specified channel. Before the START command is input, the phrase to be played back is specified with the FADR command. The START command is used to start the playback of multiple channels at the same time.
Input is possible when the NCR signal of the channels to be played back is at the "H" level.
The settings for C1and C0 are as shown in the table below.

C1	C0	Description
0	1	Starts to play back channel 1.
1	0	Starts to play back channel 2.

Multiple channels can be set at the same time.

The diagram below shows the timing for playing back channels 1 and 2 at the same time.



7. FADR Command

• command

0	1	1	0	0	0	C1	C0	1st byte
F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

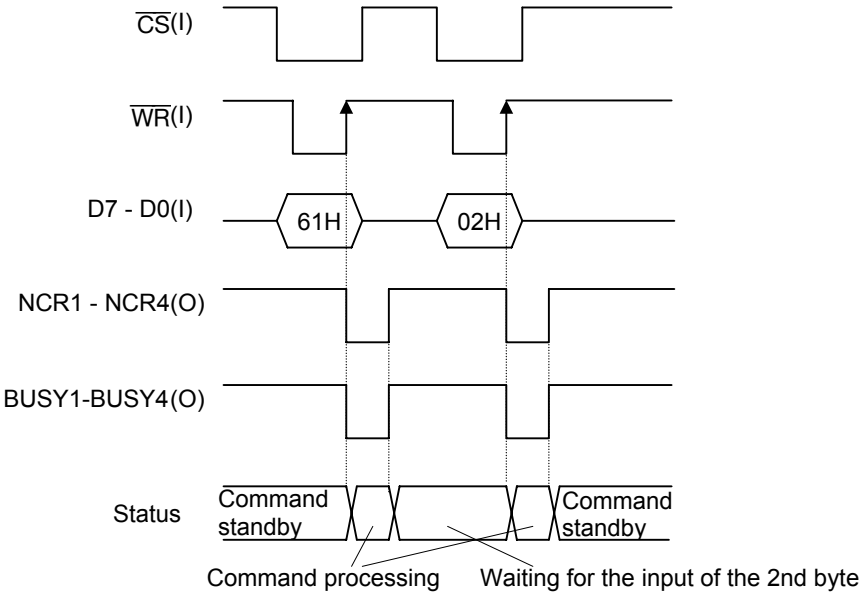
The FADR command is a two-byte command. First it specifies the channel and then it sets the phrase to be played back. After setting the phrase to be played back for each channel, it starts playback with the START command. Input is possible when the NCR signal of the specified channel is at the "H" level.
The settings for C1and C0 are as shown in the table below.

C1	C0	Description
0	1	Sets the phrase for channel 1.
1	0	Sets the phrase for channel 2.

Multiple channels can be set at the same time.

The phrases to be played back (F7-F0) can be specified when the ROM for storing the voice data is created, so set the phrases that are set when creating the ROM.

The diagram below shows the timing for specifying (F7-F0) = 02H as the phrases to play back on channel 1.



If different phrases are played back with the PLAY command, the phrase previously set by the FADR command will be changed to the phrase played back by the PLAY command, so use the FADR command again to set the phrase to be played back.

8. STOP Command

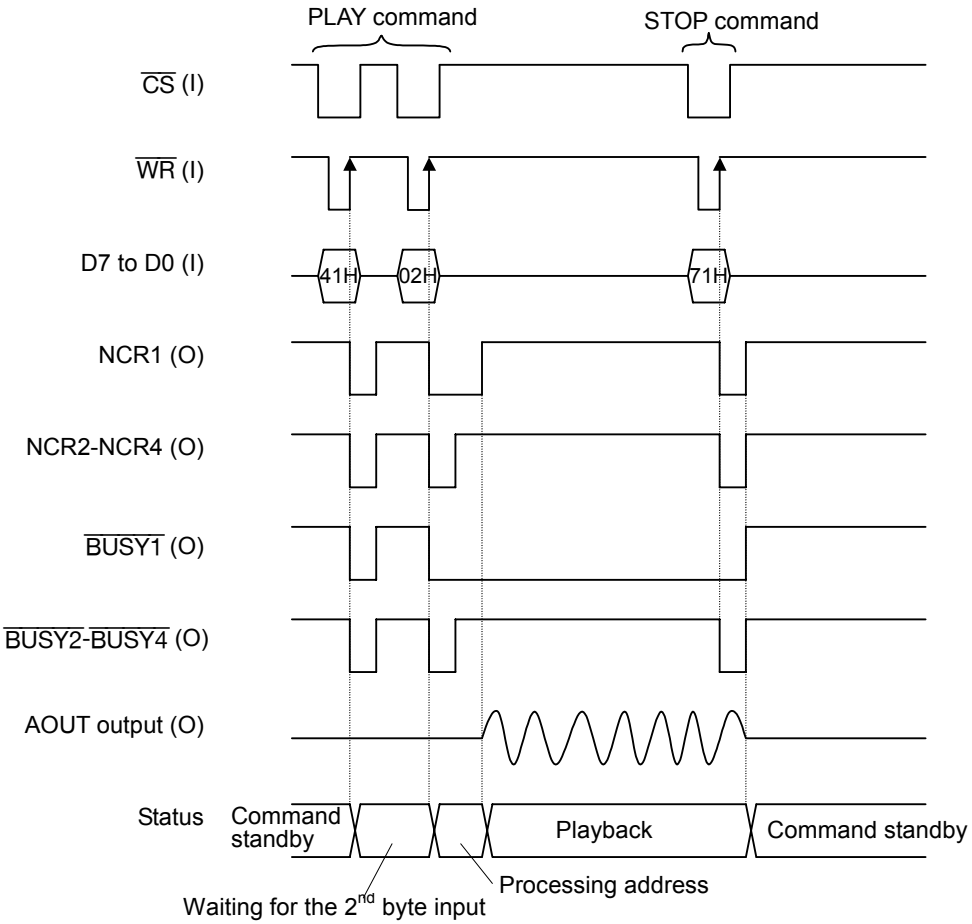
• command	0	1	1	1	0	0	C1	C0

STOP command is used to stop playback on channel(s) that correspond to C1 and C0. When the speech synthesis processing stops, the AOUT output of that channel becomes $1/2V_{DD}$ and the NCRn and BUSYn signals go "H".
Although it is possible to input the STOP command regardless of the status of playing back NCRn, a prescribed command interval time is necessary.
Note that STOP command input during power down, shifting to power up, and shifting to power down will be ignored.

C1 and C0 settings are described below.

C1	C0	Description
0	1	Stops channel 1 playback.
1	0	Stops channel 2 playback.

Multiple channels can be set at the same time.



9. MUON Command

• command

1	0	0	0	1	0	C1	C0	1 byte
M7	M6	M5	M4	M3	M2	M1	M0	2 bytes

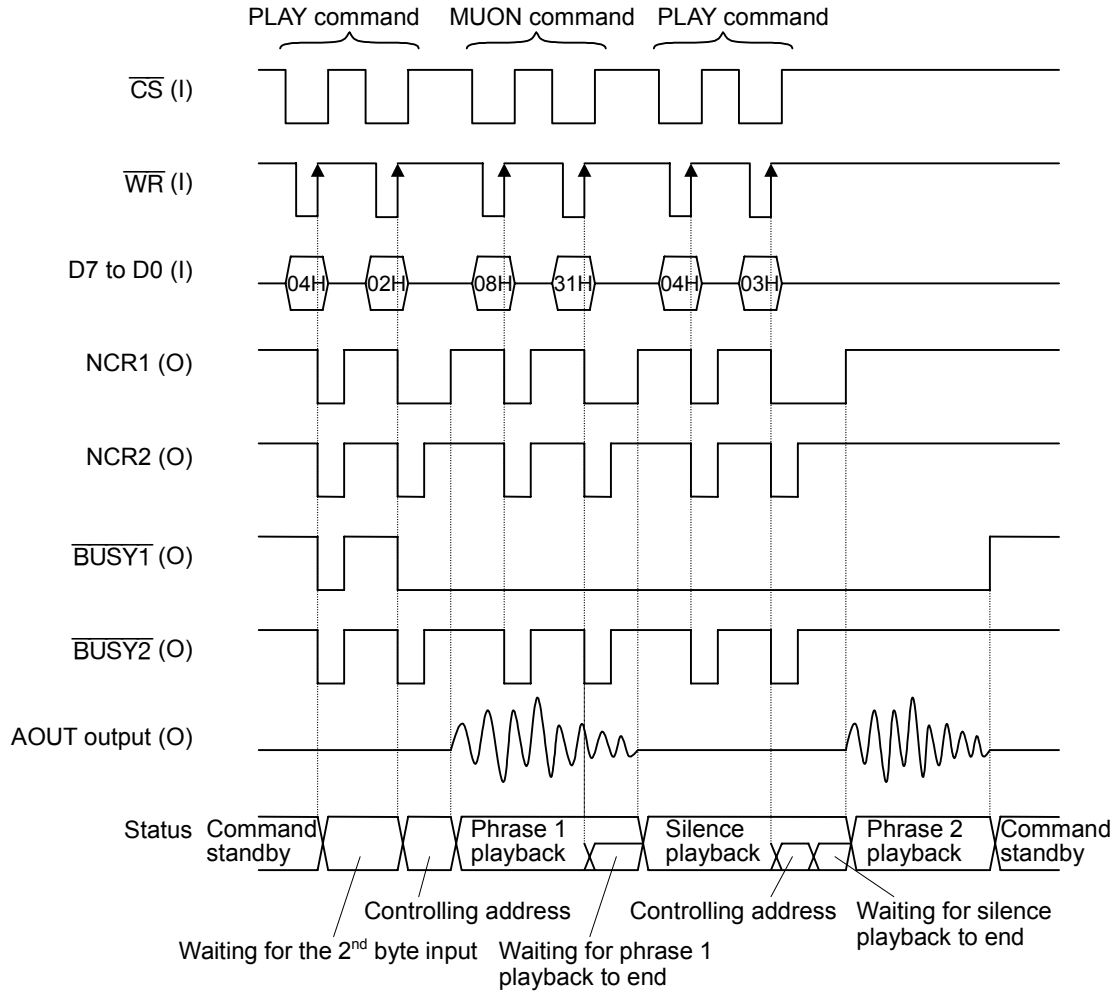
MUON command is a 2-byte command. This command is used to insert silence between the 2 playback phrases. First is specified the channel in which silence is to be inserted and next is set the silence time length.

C1	C0	Description
0	1	Inserts silence in channel 1.
1	0	Inserts silence in channel 2.

The silence length (M7 to M0) can be set in 256 steps between 4 ms and 1024 ms in 4 ms intervals.
Following is the equation to set the silence time length:

$$t_{mu} = (2^7 \times (M7) + 2^6 \times (M6) + 2^5 \times (M5) + 2^4 \times (M4) + 2^3 \times (M3) + 2^2 \times (M2) + 2^1 \times (M1) + 2^0 \times (M0) + 1) \times 4 \text{ ms}$$

The timing diagram shown below is a case of inserting a silence of 200 ms between the 2 phrases of address (F7 to F0 = 02H) and address (F7 to F0 = 03H) on channel 1.



When the PLAY command is input, the address control of phrase 1 ends, the phrase playback starts, and the NCR1 signal goes “H” level. The MUON command is input after this NCR1 signal changes to the “H” level. After the MUON command input, the NCR1 signal remains at “L” level up to the end of phrase 1 playback, and the device enters into a state waiting for the phrase 1 playback to end.
When the phrase 1 playback finishes, the silence playback starts, and NCR1 signal goes “H” level. The PLAY command that specified the next playback phrase 2 is input after this NCR1 signal has changed to the “H” level.
After the PLAY command input, the NCR1 signal once again returns to “L” level and the device enters the state waiting for phrase 2 address control and the end of silence playback.
When the silence playback finishes, the phrase 2 playback starts, the NCR1 signal goes “H” level, and the device enters a state in which it is possible to input the next PLAY or MUON command.
BUSY1 signal remains “L” level from input of the phrase 1 PLAY command up to the end of phrase 2 playback.

10. SLOOP Command

• command	1	0	0	1	0	0	C1	C0

The SLOOP command is used to repeatedly play back the voice of a designated channel. The CLOOP command is used to release the repeated playback setting.
Since the SLOOP command is valid only for a channel on which the playback is going on, make sure to input the SLOOP command after the PLAY command input.

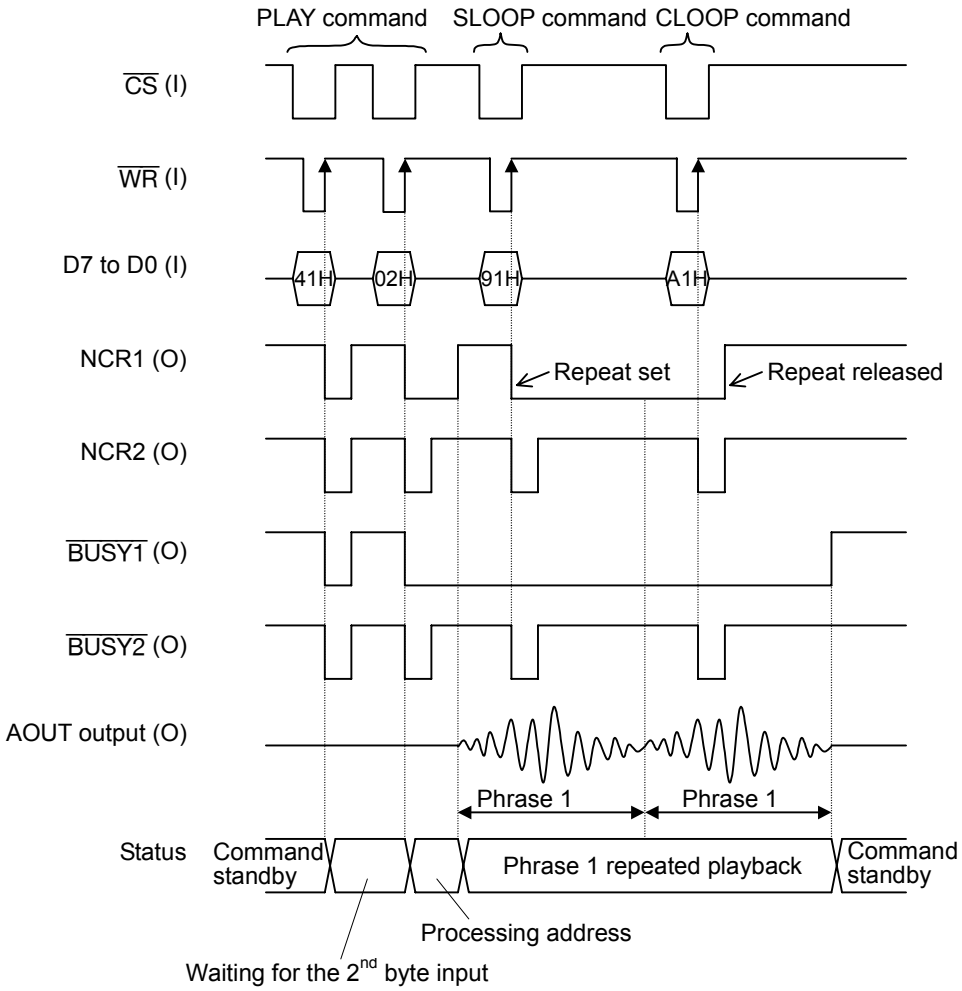
C1 and C0 settings are described below.

C1	C0	Description
0	1	Repeatedly plays back channel 1.
1	0	Repeatedly plays back channel 2.

Multiple channels can be set at the same time.

If C1 and C0 corresponding to a channel are set to “H” by SLOOP command, then the current playback phrase will be repeatedly played back. Input SLOOP command when NCRn = “H”. NCRn is “L” level while the LOOP playback is being set.
Once “H” is set to C1 and C0, the voice is repeatedly played back until the repeated playback setting is released by SLOOP command, or stop playback by the STOP command. Since the repeated playback is released when the STOP command is input, input the SLOOP command once again if desired to repeat the playback. In the case of a phrase using the edit function, the edited phrase is repeatedly played back.

Figure below shows the timing diagram to repeat the playback on channel 1.



SLOOP Command Input Scope

The SLOOP command must be input following the playback start command (PLAY or START command) and after the NCR signal of the channel to be played back has reached the "H" level, but before its BUSY signal reaches the "H" level. If the SLOOP command is input in this interval, it is effective and repetitive play is performed.

However, if the SLOOP command is input near the end of phrase playback, silence is inserted between the first repetitive phrases. The reason for this is the same for repetitive playback as for normal continuous playback. If the SLOOP command is input after there are too few sampling periods of voice data remaining in the phrase that is playing back to allow for the address management of the next phrase, the next phrase (the same phrase as the one currently playing back) cannot start immediately. Silence is inserted to allow time for the address management of the second phrase to be completed before it can start to playback.

The input timing of the SLOOP in which no silence is inserted between repetitive phrases is the same as the input timing of the PLAY/START commands in which no silence is inserted between the phrases at time of continuous playback, as shown in the table below.

Playback method	SLOOP input timing Amount of remaining voice data in playing back phrase
2 bit Oki ADPCM2	69th sample or before
4 bit Oki ADPCM2	35th sample or before
8 bit nonlinear / 8 bit PCM	18th sample or before
16 bit PCM	18th sample or before

If the SLOOP command for the second phrase is input before the number of samples indicated in the table is reached, repetitive playback is achieved without the need to insert silence between phrases.

In any case, from the second repetition on there is no insertion of silence.

11. CLOOP Command

• command	1	0	1	0	0	0	C1	C0

The CLOOP command releases the repetitive playback mode for the specified channel.
When the repetitive playback mode is released, the NCRn goes to the "H" level.
It is possible to input the CLOOP command regardless of the status of the NCRn of the channel that is playing back, but the prescribed command interval is required.

The settings for C3-C0 are as shown in the table below.

C1	C0	Description
0	1	Releases the repetitive mode for channel 1.
1	0	Releases the repetitive mode for channel 2.

Multiple channels can be set at the same time.

CLOOP Command Input Timing

Depending on the timing of the CLOOP command input during repetitive playback, the repetitive playback will end either at the end of the currently playing back phrase or after one more repetition of the phrase.

The difference is due to the same process that is required for repetitive playback and normal continuous playback. If the CLOOP command is input at a point in the phrase where the remaining voice data is less than the number of sampling periods required for address management, the address management of the next phrase to be played back (in this case, the same phrase) will have already begun. As the conclusion of address management automatically starts the next phrase playback, the CLOOP command will not take effect until that repetition is complete.

The input timing of the CLOOP command that is necessary to release repetitive playback without the final repetition is the same as the input timing for the PLAY/START commands in which no silence is inserted between the phrases at the time of continuous playback, as shown in the table below.

Playback method	CLOOP input timing Amount of remaining voice data in playing back phrase
2 bit Oki ADPCM2	69th sample or before
4 bit Oki ADPCM2	35th sample or before
8 bit nonlinear / 8 bit PCM	18th sample or before
16 bit PCM	18th sample or before

If the CLOOP command for the second phrase is input before the number of samples indicated in the table is reached, repetitive playback ends at the end of the currently playing back phrase.

12. VOL Command

• command

1	0	1	1	0	0	C1	C0	1 byte
0	0	0	V4	V3	V2	V1	V0	2 bytes

VOL command is used to adjust the volume of a channel set by CH. The volume can be set in 29 steps up to –58 dB: –2 dB step up to –50 dB, and –5 dB step after –50 dB.

C1	C0	Description
0	1	Sets volume of channel 1.
1	0	Sets volume of channel 2.

Following are the volume settings (V4 to V0):

V4	V3	V2	V1	V0	Volume	V4	V3	V2	V1	V0	Volume
0	0	0	0	0	0 dB	1	0	0	0	0	–32 dB
0	0	0	0	1	–2 dB	1	0	0	0	1	–34 dB
0	0	0	1	0	–4 dB	1	0	0	1	0	–36 dB
0	0	0	1	1	–6 dB	1	0	0	1	1	–38 dB
0	0	1	0	0	–8 dB	1	0	1	0	0	–40 dB
0	0	1	0	1	–10 dB	1	0	1	0	1	–42 dB
0	0	1	1	0	–12 dB	1	0	1	1	0	–44 dB
0	0	1	1	1	–14 dB	1	0	1	1	1	–46 dB
0	1	0	0	0	–16 dB	1	1	0	0	0	–48 dB
0	1	0	0	1	–18 dB	1	1	0	0	1	–50 dB
0	1	0	1	0	–20 dB	1	1	0	1	0	(–50 dB)
0	1	0	1	1	–22 dB	1	1	0	1	1	–55 dB
0	1	1	0	0	–24 dB	1	1	1	0	0	(–55 dB)
0	1	1	0	1	–26 dB	1	1	1	0	1	–60 dB
0	1	1	1	0	–28 dB	1	1	1	1	0	(–60 dB)
0	1	1	1	1	–30 dB	1	1	1	1	1	OFF

All channels are set to 0 dB at the power insertion and RESET input.

13. EXT Command

• command

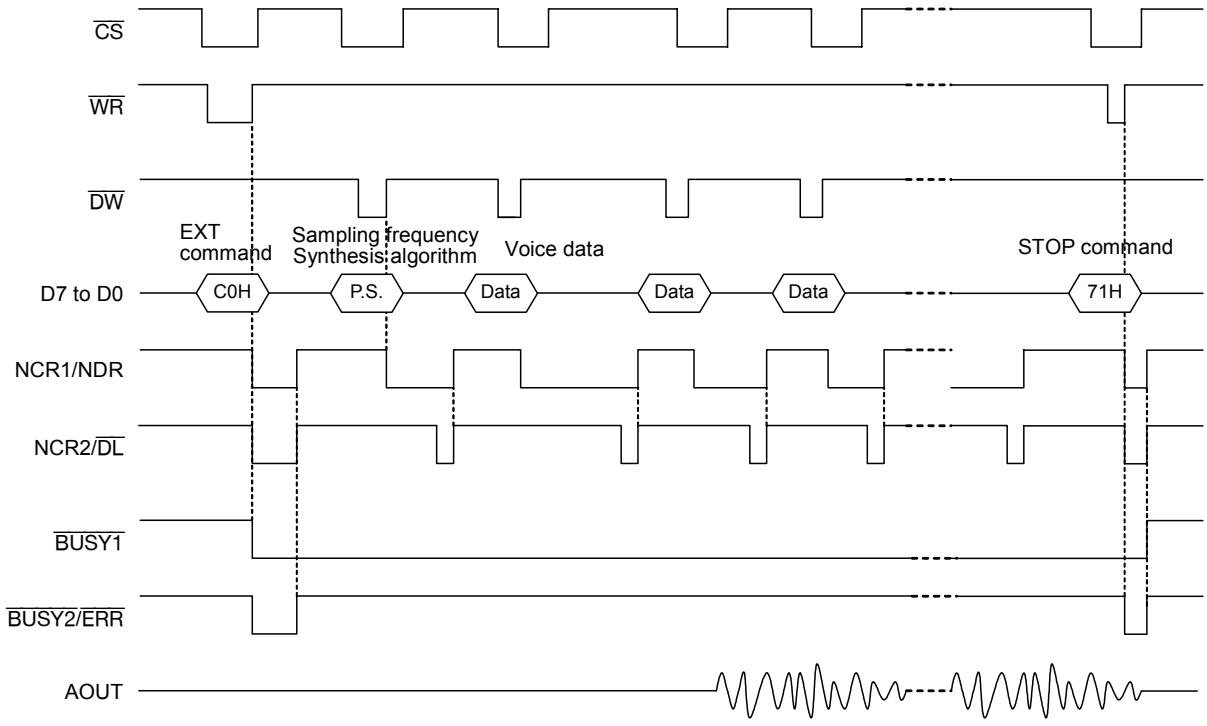
1	1	0	0	0	0	0	0

EXT command is used to play back an external voice data other than the built-in ROM. Since the playback uses channel 1, specify channel 1 when inputting the STOP and VOL commands.
Note that commands other than the STOP and VOL inputs during the playback by EXT command will be ignored. Also, the EXT command input during the built-in ROM playback will be ignored.
Channel mixing is not possible when executing the EXT command.
Table below describes the function of each pin when the EXT command is executed.

• Parallel Input Interface

Pin	Type	Function
D7 to D0	I	External data input pins.
$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ = "H", the $\overline{WR}$ and $\overline{DW}$ signals cannot be input to the device.
$\overline{DW}$	I	Voice data write pin. Input data to this pin when NCR1/NDR pin is at "H" level.
NCR2/$\overline{DL}$	O	Works as $\overline{DL}$ pin when executing EXT command. Outputs signal which the device uses to capture the input data. The data is captured inside with the rising edge.
NCR1/NDR	O	Works as NDR pin when executing the EXT command. When NDR= "H", the voice data can be input.
$\overline{BUSY2}$/$\overline{ERR}$	O	Works as $\overline{ERR}$ pin when executing the EXT command. When inputting voice data if any error occurs in the transfer of data, this pin outputs "L" level and the voice output may become noisy.

Figure below shows the timing diagram when executing the EXT command (16-bit PCM is excluded).



When the EXT command is input, after the elapse of the command processing time, the device waits for input of setting data of sampling frequency and voice synthesis algorithm.
When the setting data of sampling frequency and voice synthesis algorithm has been input, the NDR signal goes "L" level and sets the sampling frequency and voice synthesis algorithm with the rising edge of DL signal. The NDR signal goes "H" with the rising edge of this DL signal and the device enters into a state waiting for the voice data input.
When the voice data is input, the NDR signal goes "L" and the voice data is captured inside with the rising edge of DL signal, and the speech synthesis starts. The NDR signal goes "H" level with the rising edge of this DL signal, and the device waits for the input of the next voice data.
After this, the voice data is input when NDR signal is at "H" level.
After the last voice data has been input, the STOP command is input when the NDR signal has gone "H". This ends the external voice data playback mode.
To forcibly end the playback midway, it is possible to input the STOP command regardless of the state of NDR signal.

In case the prescribed data could not be input up to the rising edge of DL signal, the ERR signal goes "L" level in synchronization with the rising edge of DL signal, and informs the occurrence of an abnormality. If the ERR signal has gone "L" level once, the signal remains at "L" level until the STOP command is input.

Correspondence among the sampling frequencies, playback method, and D7 to D0 is shown below.

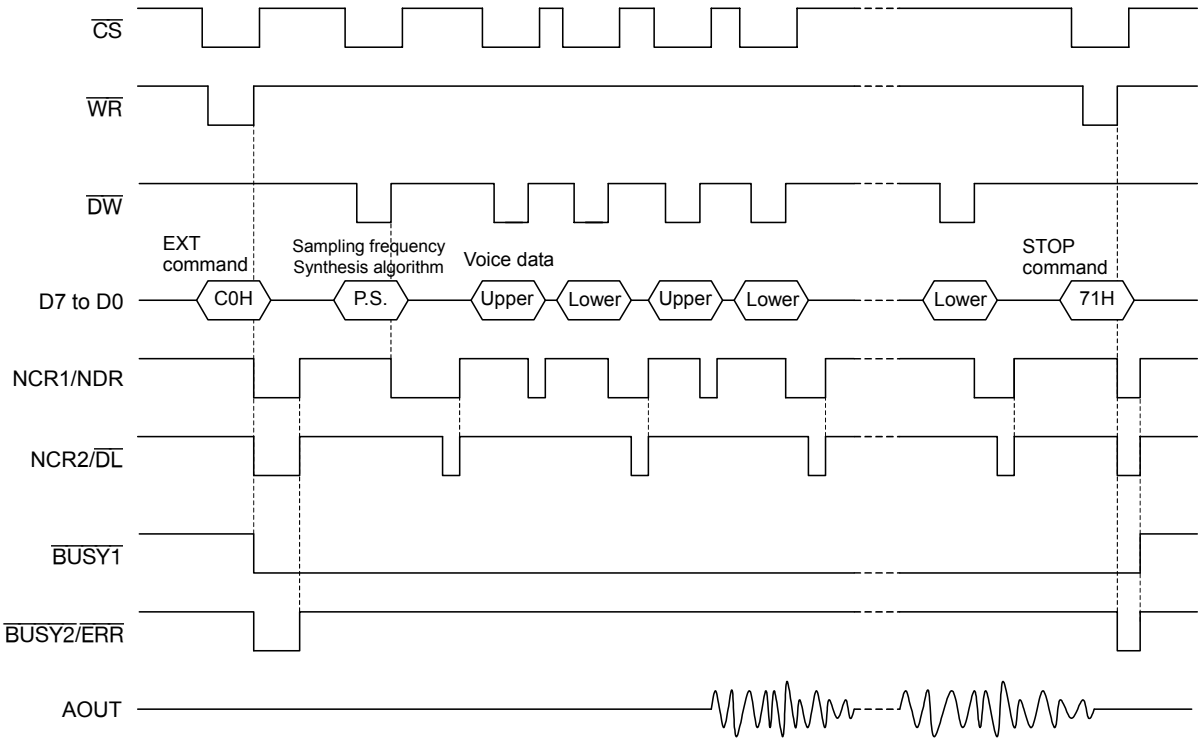
D7	D6	D5	D4	D3	D2	D1	D0
0	P2	P1	P0	S3	S2	S1	S0

P2 to P0: Playback method
S3 to S0: Sampling frequency

P2	P1	P0	Playback method
0	0	0	2-bit ADPCM2
0	0	1	4-bit ADPCM2
0	1	0	8-bit non-linear PCM
0	1	1	8-bit PCM
1	0	0	16-bit PCM
1	0	1	Not used
1	1	0	Not used
1	1	1	Not used

S3	S2	S1	S0	Sampling frequency
0	0	0	0	4.0 kHz
0	0	0	1	8.0 kHz
0	0	1	0	16.0 kHz
0	0	1	1	32.0 kHz
0	1	0	0	5.3 kHz
0	1	0	1	10.7 kHz
0	1	1	0	21.3 kHz
0	1	1	1	42.7 kHz
1	0	0	0	6.4 kHz
1	0	0	1	12.8 kHz
1	0	1	0	25.6 kHz
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	48.0 kHz

Figure below shows a timing diagram when executing the EXT command (16-bit PCM).



In the 16-bit PCM playback, the upper 8 bits in the 16-bit voice data are input first. NDR signal goes “L” level when the upper 8-bit data is input. When the device captures the data, the NDR signal goes “H” level. The data capture internal signal at this time does not appear on DL signal, and the DL signal remains at “H” level.
The lower 8 bits in16-bit voice data are input after the NDR signal has gone “H” level. When the lower 8-bit data is input, the NDR signal goes “L” level, and the 16-bit voice data is captured inside with the rising edge of DL signal to perform the speech synthesis.

14. Flash I/F Command (Applies to the ML22Q54/Q58)

• command	1	1	0	1	BE	SE	WR	RD

Flash I/F command is used to read/write/erase data on the on-chip 4-Mbit/8-Mbit flash memory. Use it for collectively rewriting of voice data. Flash I/F command cannot use during playing back. In addition, the maximum number of times to rewrite is not prescribed. The typical is 100 times.

Settings of each bit of the Flash I/F command are described below.

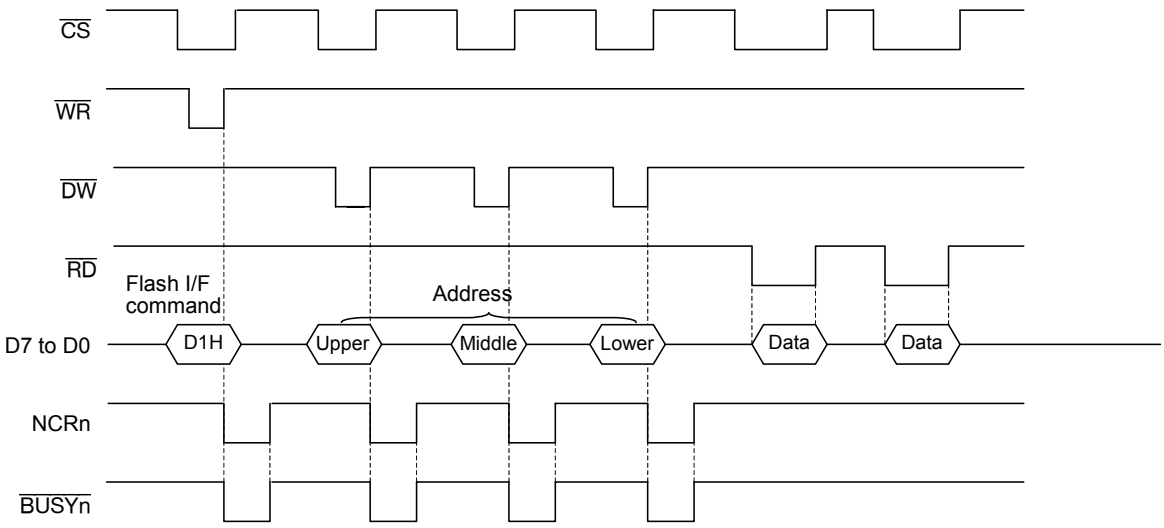
BE	SE	WR	RD	Description
0	0	0	1	Reads data.
0	0	1	0	Writes data.
0	1	0	0	Erases in sector (2-kbyte) unit.
1	0	0	0	Erases in block (64-kbyte) unit

Multiple bits cannot be set to “1”.

1) Data Read

Read address is specified from DW pin in continuation with the Flash I/F command. The RD pin goes low and, consequently, the read data is output to CPU I/F. It is possible to continuously read data because the address automatically increments with the rising edge of RD pin. To read data of a different address, input again from the Flash I/F command.

The data read mode can be exit by a command that is input from WR pin.



Note) “n” means 1 or 2.

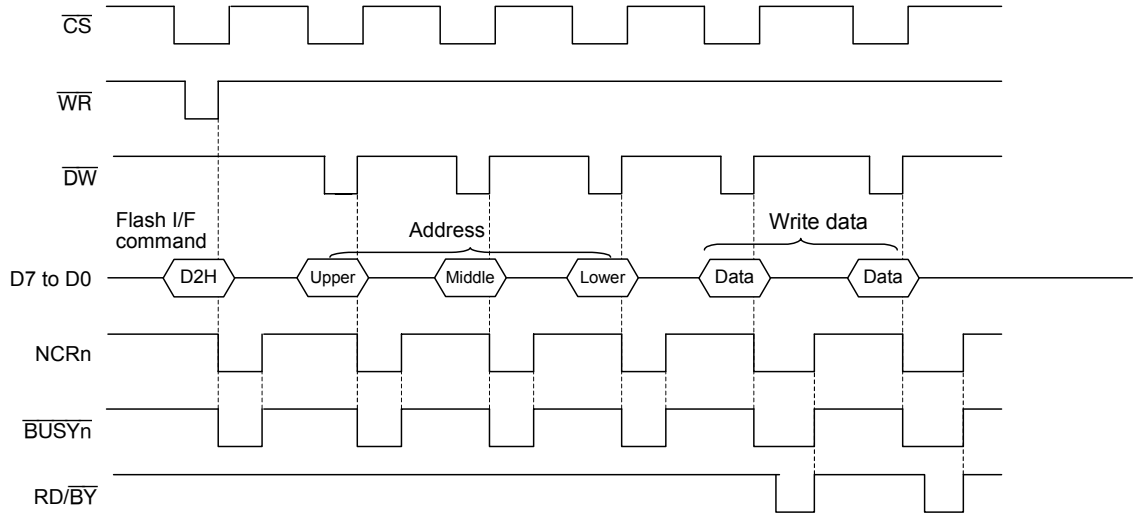
2) Data Write

Write address is specified from DW pin in continuation with the Flash I/F command. The write address is the input from the DW pin. The operation of data write to the flash memory starts automatically when the write data is input. "L" level is output at RD/BY pin during the operation of data write to the flash memory.

At the end of the data write operation, the RD/BY signal goes "H" level, and NCR and BUSY signals also go "H" level. At this time, the address increments automatically and the device enters the state waiting for the next write data input.

In the case of writing data to a different address, input again from the Flash I/F command.

It is possible to exit from the data write mode by a command that is input from WR pin. Notice that all commands input during the "L" level of the NCR or BUSY signal will be ignored.



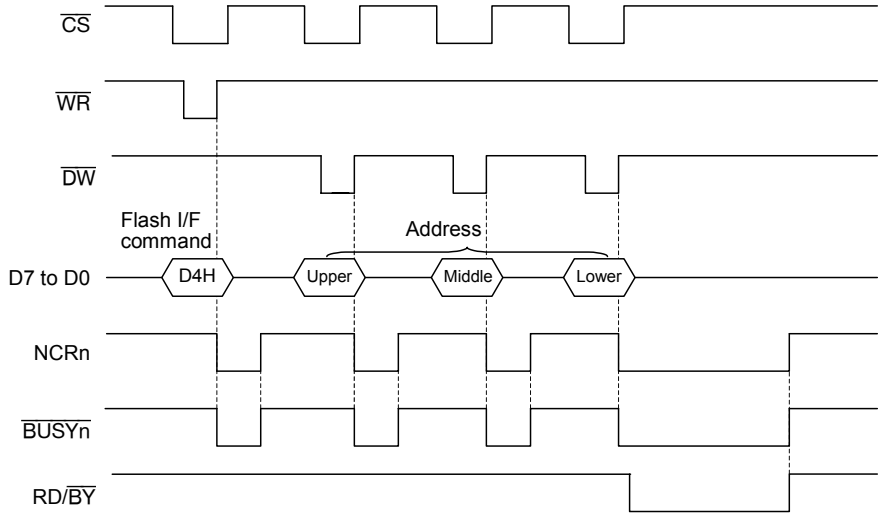
Note) "n" means 1 or 2.

3) Data Erase

The erase address is input from DW pin in continuation with the Flash I/F command. When the erase address is input, the data erase operation of the flash memory starts automatically. “L” level is output at RD/BY pin during the flash memory erase operation.

At the end of the address erase operation, RD/BY signal goes “H” level, and the NCR and BUSY signals also go “H” level at the same time. Since the address is not incremented in the erase operation, input again from the Flash I/F command in the case of erasing a different address. The operations are the same to erase a sector and to erase a block.

Notice that all commands input while either NCR signal or BUSY signal is “L” level will be ignored.



Note) “n” means 1 or 2.

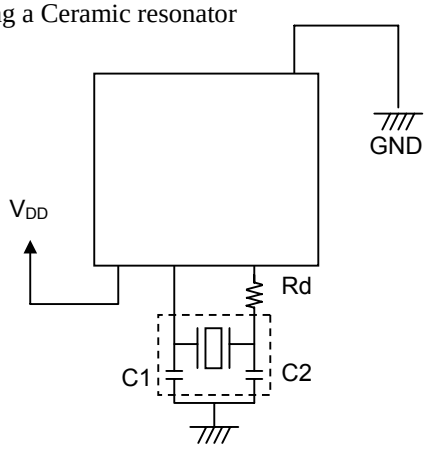
RECOMMENDED CERAMIC OSCILLATION

The optimal load capacities when connecting ceramic resonators from KYOCERA CORPORATION, TDK CORPORATION and MURATA MFG., are shown below for reference.

KYOCERA

Freq [Hz]	Type	Optimal load capacity					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply Voltage Range[V]	Operating Temperature Range[°C]
4.0M	PBRC4.00GR	30(external)		---	1.0k	2.7 to 5.5	-40 to +85*
	PBRC4.00HR	30 (internal)					

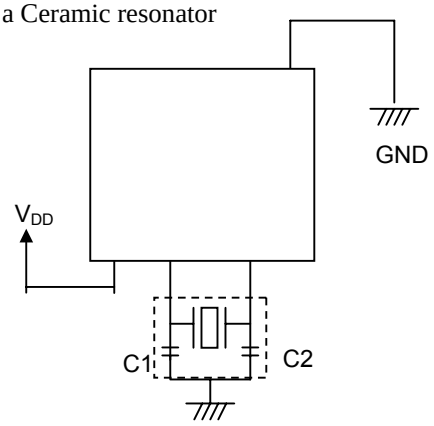
Oscillation circuit diagram using a Ceramic resonator



TDK CORPORATION

Freq [Hz]	Type	Optimal load capacity					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply Voltage Range[V]	Operating Temperature Range[°C]
4.0M	FCR4.0MC5	30 (internal)		---	---	2.7 to 5.5	-40 to +85*

Oscillation circuit diagram using a Ceramic resonator

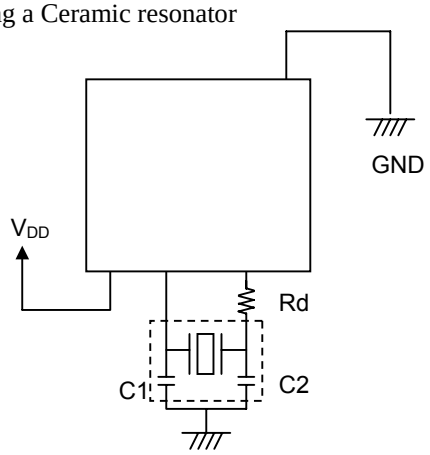


* Operating temperature of ML22Q54/Q58 is 0 to +70.

MURATA MFG.,

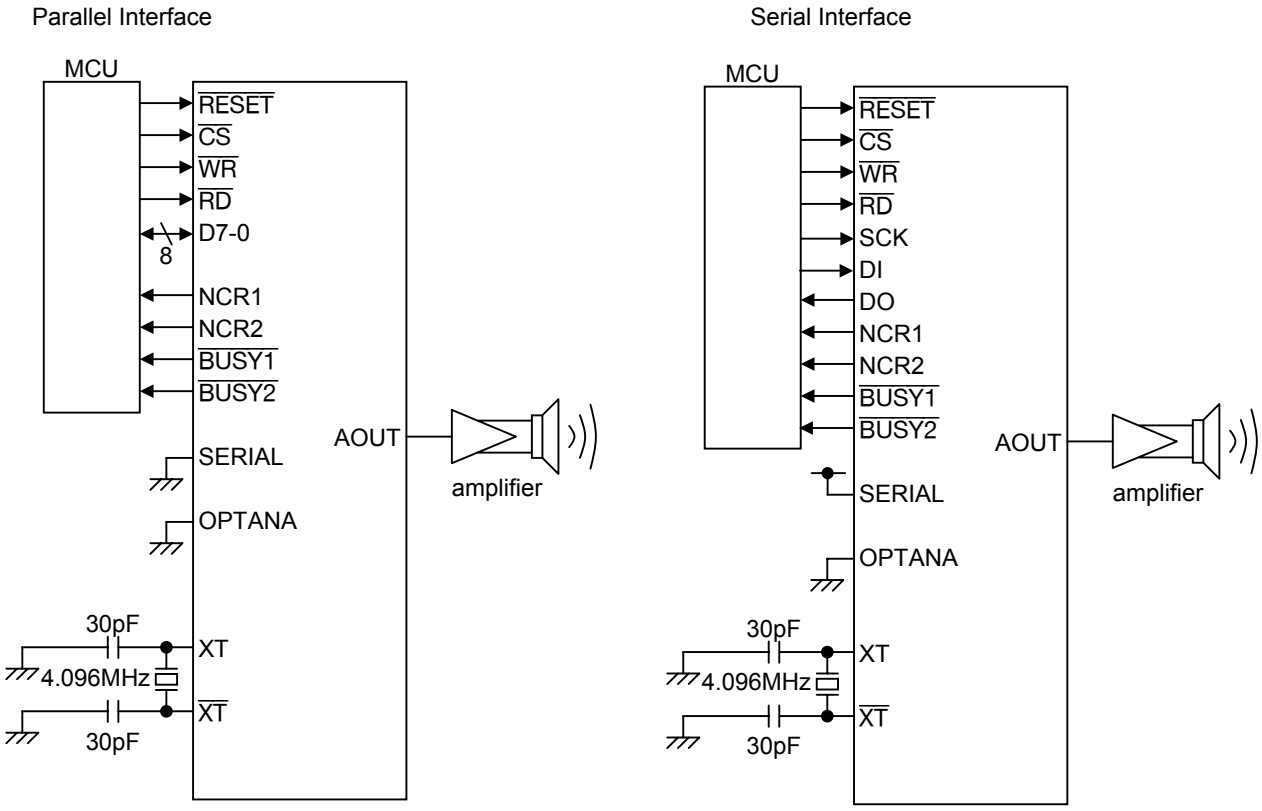
Freq [Hz]	Type	Optimal load capacity					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply Voltage Range[V]	Operating Temperature Range[°C]
3.500M	CSTCC3M50G56-R0	47 (internal)		---	1.5k	2.7 to 5.5	-40 to +85*
	CSTLS3M50G56-B0	47 (internal)					
4.096M	CSTCR4M09G55-R0	39 (internal)		---	1.0k	2.7 to 5.5	
	CSTLS4M09G56-B0	47 (internal)					
4.500M	CSTCR4M50G55-R0	39 (internal)		---	1.0k	2.7 to 5.5	
	CSTLS4M50G56-B0	47 (internal)					

Oscillation circuit diagram using a Ceramic resonator



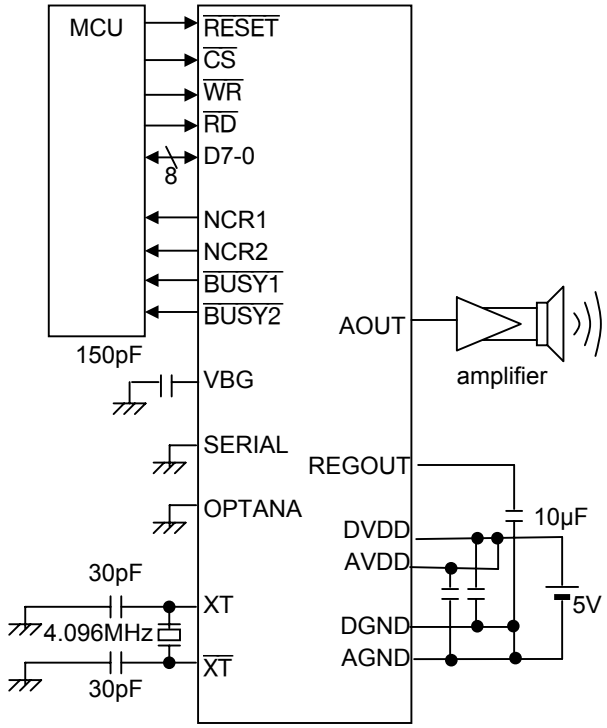
* Operating temperature of ML22Q54/Q58 is 0 to +70.

APPLICATION CIRCUIT EXAMPLE (ML2251/52/53/54/56-XXX, ML22Q54)

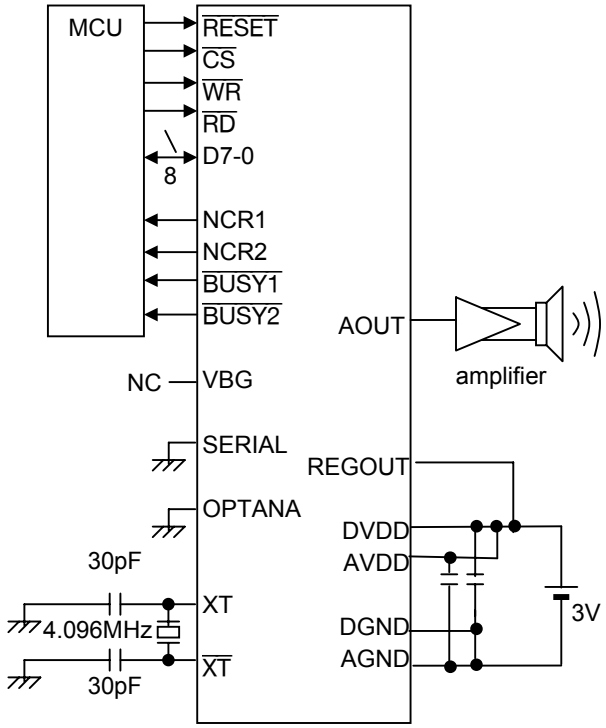


APPLICATION CIRCUIT EXAMPLE (ML22Q58)

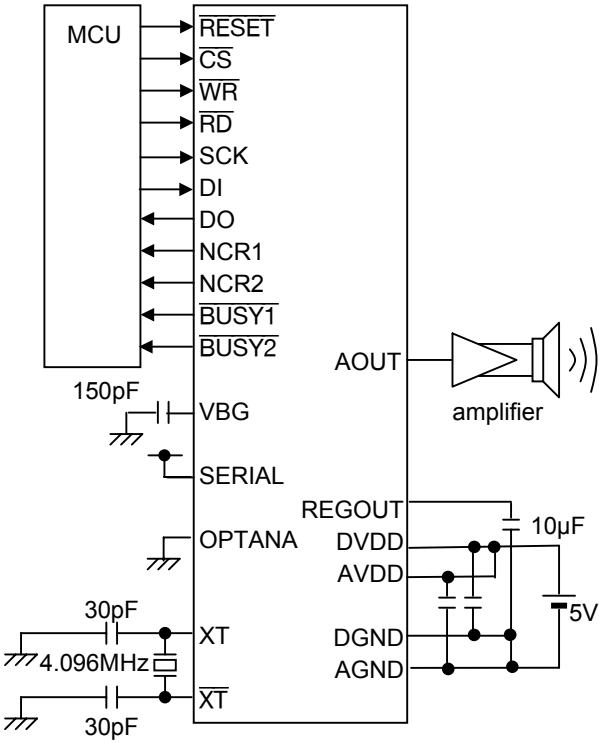
Parallel Interface (at 5V)



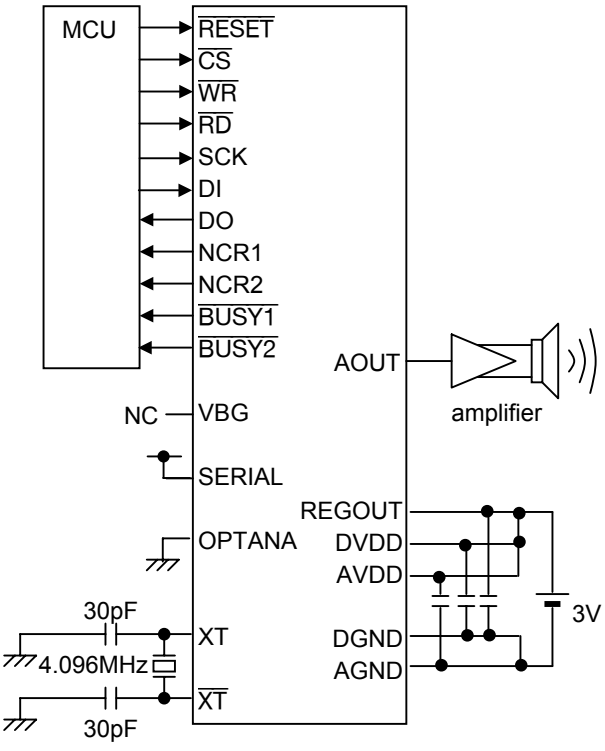
Parallel Interface(at 3V)



Serial Interface (at 5V)



Serial Interface (at 3V)

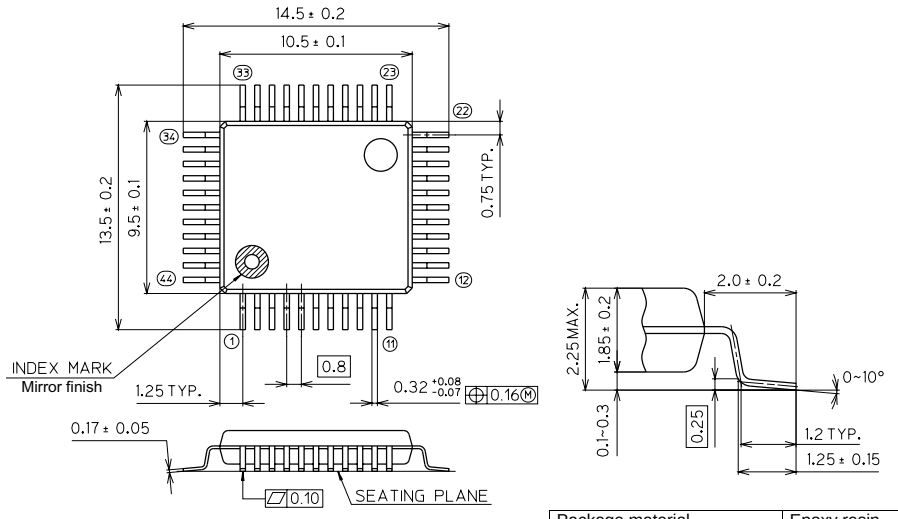


PACKAGE DIMENSIONS

44pin plastic QFP

(Unit: mm)

QFP44-P-910-0.80-2K



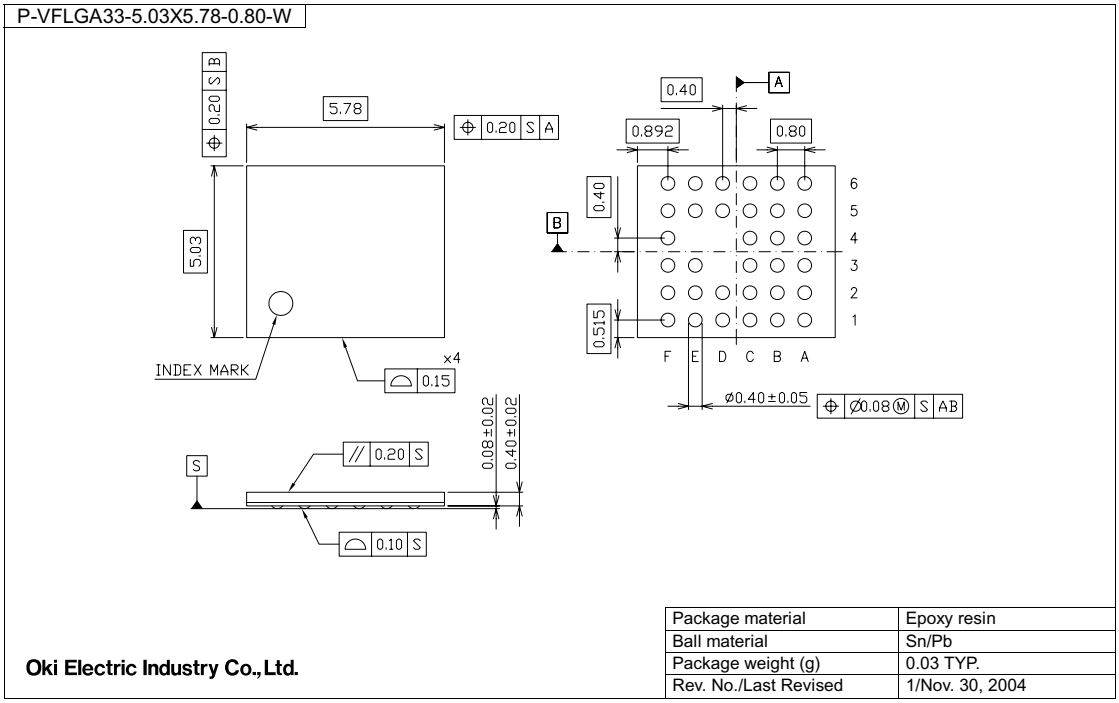
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

33-pin W-CSP



Package material	Epoxy resin
Ball material	Sn/Pb
Package weight (g)	0.03 TYP.
Rev. No./Last Revised	1/Nov. 30, 2004

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL2250FULL-01	Jun. 25, 2002	–	–	Preliminary edition 1
FEDL2250FULL-01	Oct. 15, 2002	–	–	Final edition 1
FEDL2250FULL-02	May 12, 2003	–	–	Final edition 2
FEDL2250FULL-03	Oct. 17, 2003	–	–	Added ML2251 and ML2253
		–	–	Eliminated mentioned items about PWM
FEDL2250FULL-04	Apr. 20, 2004	–	–	Added ML2256
		49	49	Added mentioned items about initial state at reset input
FJDL2250FULL-06	2004.12.27	-	-	Added ML22Q58
		-	10-12, 87	Added ML2253/54-XXXHB(W-CSP Package)
		-	16-18	Added the pin equivalent circuits
		44,45	50, 51	Corrected the airticle and charts about serial Interface
		-	65	Added notes for continuous play
		-	82, 83	Added recommended ceramic oscillation
		73	84, 85	Changed the application circuit example

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